2019

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Shahab Sajedi

Technological University Dublin, shahab.sajedi@tudublin.ie

Michael Farrell

Technological University Dublin, michael.farrell@tudublin.ie

Malabika Basu

Technological University Dublin, malabika.basu@tudublin.ie

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Recommended Citation

Shahab Sajedi, Michael Farrell, Malabika Basu, DC side and AC side cascaded multilevel inverter topologies: A comparative study due to variation in design features, International Journal of Electrical Power & Energy Systems, Volume 113, 2019, Pages 56-70, ISSN 0142-0615, DOI: 10.1016/j.ijepes.2019.05.019.

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DC side and AC side cascaded multilevel inverter topologies: A comparative study due to variation in design features

Shahab Sajedi, Michael Farrell, Malabika Basu*

Technological University Dublin, Ireland

ARTICLE INFO

Keywords:

Modular multilevel converter
High voltage direct current (HVDC)
DC Fault
Converter losses

ABSTRACT

This paper presents a comparative study between DC side and AC side cascaded topologies for the hybrid modular multilevel converter (MMC) which are becoming popular in recent years. A multilevel converter with half or full bridge sub modules connected across DC link is another alternative for high-voltage applications as it has the same number of sub modules and footprint as AC side cascaded topology with the same DC link voltage and AC side voltage. The compared AC side cascaded structure offers a two-level converter as the high voltage stage and cascaded H-bridge (which is full bridge) sub modules with electrically isolated DC sources or capacitors for the low voltage stages which has number of features suitable for HVDC application. The comparison aspects are investigated against 6 different converter sub module number and configuration options for losses, harmonic profile of the output voltage, and the DC fault current characteristics (before blocking the IGBT gate signals during the DC fault) with the same input DC voltage and the same load for both (DC and AC side) topologies. The major results and findings of this investigation are presented, compared and discussed.

1. Introduction

As greenhouse gas emissions are increasing, the use of power electronics and High-Voltage DC (HVDC) transmission could be considered as a key enabling technology for the integration of clean energy resources [1–4]. In recent years, Modular Multilevel Inverters (MMC) have received more interest because of the development of smart grids and multi-terminal HVDC networks [5–8]. The unique structure of modular multilevel inverters allow them to work with high efficiency, low harmonic distortion without using output filters, low switching frequency and good modularity to meet any voltage level requirements [9–12]. Several multilevel topologies have been proposed, including a hybrid multilevel converter with AC side cascaded H-bridge (which is full bridge) sub modules, an alternative arm modular multilevel converter and DC side cascaded multilevel with half bridge or full bridge sub modules connected across the DC link [13–15].

The hybrid multilevel converter with AC side cascaded sub modules is presented in [16–18]. This topology has DC fault blocking capability with a lower number of H-bridge sub modules and smaller footprint than the other topologies. In addition, it has a higher DC voltage utilization factor due to the use of floating capacitors as a virtual DC link for each H-bridge sub module to increase the modulation index. The main drawback of this structure is synchronization mis-match between

the two-level converter as high power stage and the H-bridge cascaded sub modules. This necessitates the use of filters to attenuate the 5th and 7th harmonics.

The hybrid multilevel converter with half bridge or full bridge sub modules connected across the DC link are investigated in [19–25]. Paper [19] investigates about the half-bridge DC side cascaded topology and analyses the pulse width modulation and capacitor voltage balancing of a three-level modular converter that uses phase voltage redundant states. In paper [20] a new hybrid cascaded modular multilevel converter is presented. The half-bridge sub modules are used on the main power stage and the cascade full-bridge (FB) sub modules are connected to its AC side. The full bridge sub module MMC is proposed in [21–24] and the DC side fault analysis of full bridge MMC is presented in [25].

Although this kind of topology with the same number of H-bridge sub modules has a similar footprint to the AC side cascaded topology, its main drawback is the voltage stress on the converter switches cannot be maintained around a specific set-point. The other issue is the hybrid multilevel converter with half bridge sub modules is unable to block DC side faults. This issue can be addressed by using full bridge instead of half bridge sub modules. However, this practice will increase the initial investment cost as well as the switching losses. However, with a trade off between cost and efficiency, the hybrid MMC consisting of half

* Corresponding author.

E-mail address: mbasu@dit.ie (M. Basu).

<https://doi.org/10.1016/j.ijepes.2019.05.019>

Received 23 October 2018; Received in revised form 1 May 2019; Accepted 7 May 2019

Available online 21 May 2019

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Fig. 1. DC side cascaded topology.

bridge and full bridge sub modules could be a promising solution [26]. The hybrid MMC may have a difficulty of sub module (SM) voltage balancing under variation of its DC bus voltage. Paper [27] proposes the new control scheme to address this issue.

Considering the above literature analysis, this paper provides a comparative study and insight in to six different commonly used design cases (2 and 4H-bridge sub modules for AC side cascaded and 8 and 16 sub module combination for half bridge and full bridge DC side cascaded topologies) according to the following categories:

- Contributions of the device losses, and hence the converter efficiency
- Output voltage harmonic profile and
- DC fault current characteristics at the initiation of a fault

The loss calculation results and voltage and power rating parameters are benchmarked against an existing operational HVDC system between Ireland and UK (East-West Interconnector) that can carry 500 MW power at 400 kV [46].

The rest of this paper is organized as follows. Section 2 introduces circuit topologies of DC side cascaded and AC side cascaded MMC and their operational principle. In Section 3 issues such as power loss analysis, output voltage harmonic profile and fault operation for these two different topologies are compared when operating under similar conditions i.e. DC input voltage of 400 kV and AC load of 500 MW. The conclusion remarks are presented in Section 4.

2. Circuit topologies and operational principle of dc side cascaded and ac side cascaded MMC

Circuit topologies and operating principle of DC side cascaded and AC side cascaded MMC are presented in this section.

2.1. DC side cascaded topology

In the DC side cascaded topology two arms form a converter phase, where the DC system is connected to the upper (P) and lower (N) sides of the phase and the three-phase AC system is connected to the middle point of each phase (A,B,C). Both arms comprise series-connected identical sub-modules (SM). The arm inductance (L_{arm}), must be connected in series with each group of sub modules in order to limit the current due to instantaneous voltage differences of the arms. The desired output AC voltages are achieved by controlling the SMs to be inserted or bypassed. As all the SMs are identical and the addition of voltages of all inserted SMs in one leg is equal to DC voltage, in order to balance the DC voltage, the number of inserted SM in one phase should be the same and equal to N (N is the number of SMs per arm) for maximum number of voltage levels:

$$n_u + n_l = N \quad (1)$$

where n_u and n_l are the number of inserted SMs in upper and lower arm respectively.

DC side cascaded topology can be designed to have fault tolerant

Fig. 2. AC side cascaded topology [17].

Table 1

Simulation parameters for AC side cascaded topology.

Parameter	Value	Parameter	Value
Number of SMs	2	4	DC bus voltage
SM capacitor voltage	100 kV	50 kV	SM capacitance
(submodule) Carrier frequency	2 kHz		Output power per phases
Main converter (2-level)	400 Hz		$\frac{500}{3}$ MW

Table 2

Simulation parameters for DC side cascaded topology.

Parameter	Value	Parameter	Value
Number of SMs in each arm	8	16	Carrier frequency
Number of Half-Bridge or Full-Bridge SMs in each arm	8	16	DC bus voltage
SM capacitor voltage	100 kV	50 kV	SM capacitance
Buffer inductor	0.5 mH		Output power per phases
			$\frac{500}{3}$ MW

capability if full bridge sub modules are used in the upper and lower arms of the phase. With full bridge sub module design it is possible to suppress both DC side and AC side fault currents. The DC side cascaded topology with half bridge sub modules also can be used in the HVDC application however as it does not have fault tolerant capability a fast DC circuit breaker is needed. Fig. 1 shows the structure of DC side cascaded MMC. There are several power sub module topologies proposed in the literature. So the level of output voltage is decided by the difference between the number of inserted SMs in upper and lower arm. The number of phase voltage levels for a MMC with N SMs per arm is $N + 1$ and $2N + 1$ levels for line voltages. Consequently, the change of output voltage level of MMC is achieved by altering the state of only a few SMs, so the switching frequency is dramatically reduced.

2.1. AC side cascaded topology

Fig. 2 depicts the structure of AC side cascaded topology with N sub modules per phase. It can generate $4N + 1$ voltage levels at each converter output phase relative to imaginary supply mid-point, with predetermined voltage steps equal to one H-bridge capacitor voltage. During steady state operation, voltage stress on switching part of the two-level inverter is V_{DC} and switching part of each H-bridge sub module will experience voltage stress of $\frac{1}{2}(\frac{V_{DC}}{N})$. The two-level converter

Fig. 3. Per phase conduction losses and switching losses for AC side cascaded topology with 2 and 4 full bridges on the AC side.

Fig. 4. Per phase conduction losses and switching losses for DC side cascaded topology with 8 and 16 half bridge sub modules (SM).

is the main power stage that controls the fundamental voltage using selective harmonic elimination and the cascaded H-bridge sub modules in each phase represent a series active filter that injects harmonic voltages to attenuate those inherent in the two-level converter output voltage. The final modulation signal for H-bridge sub modules will be the difference between the target fundamental voltage and two-level converter output voltage (chopped square waveform) as shown in

Fig. 2. As the waveform across the H-bridge sub modules does not contain a fundamental voltage component, its interaction with the fundamental will not result in active power exchange between H-bridge sub modules and the AC side. Using selective harmonic elimination at the two-level converter stage will minimize the switching losses and the dc-link voltage utilization will be increased [28]. In this topology, H-bridge sub modules are cascaded on the AC side of two-level converter.

Fig. 5. Per phase conduction losses and switching losses for DC side cascaded topology with 8 and 16 full bridge sub modules (SM).

Fig. 6. Loss analysis for the seven different case studies.

This kind of topology has fault tolerant capability during AC side and DC side faults.

3. Comparison of topologies at the same input DC voltage level and the same AC load conditions

Several operational issues of the mentioned topologies such as loss analysis, output voltage harmonic profile and the DC fault current analysis before the blocking of the IGBTs occurs will be discussed in this section.

3.1. Comparison of the losses between DC side cascaded and AC side cascaded topologies

This section introduces a loss and efficiency calculation for the half bridge sub module DC side cascaded, full bridge sub module DC side cascaded and AC side cascaded topologies at the same input DC voltage level and the same AC load. Several studies prove that the DC side cascaded topology has a higher efficiency than the other multilevel topologies because of the internal current controllability to minimize the losses [29]. There are several methods of loss calculation for the MMC: e.g. calculation using adjustment of switching waveforms [30], calculation using the linear interpolation and semiconductor energy

Fig. 7. Output voltage for single phase AC side cascaded topology with two H-bridges.

Fig. 8. Harmonic spectra of output voltage for AC side cascaded topology with two H-bridges.

[31] and using real-time waveforms and temperature feedback [32].

There are four different types of loss for any kind of power electronics device which are: (1) Conduction losses, (2) Switching losses, (3) OFF-state losses and (4) Gate losses [33]. The Off-state and Gate losses are very small and normally neglected. Hence, in this paper, only conduction and switching losses have been considered for the comparative analysis. Paper [34] presents the exact method for the inverter losses calculation. However, loss calculation for high power rated inverters are to be customised because of the number of series switches to withstand nominal voltage and parallel switches to withstand the rated current needs to be precisely considered. Computer simulation is one of the powerful methods to calculate and evaluate the losses in a MMC converter. In this case the accuracy of loss calculations depends on how well the computer model is designed to reflect the real world conditions.

The on-state voltage drop in the device produces the conduction losses. These losses are computed by averaging the conduction losses in each switching cycle as shown in Eq. (2) where f_s is the switching frequency and $w=2\pi f_s$:

$$P_{cond} = \frac{1}{T} \int_0^T V_f(wt) i(wt) dwt \quad (2)$$

where P_{cond} shows the conduction losses of the device, $V_f(wt)$ shows the forward voltage drop of the device and $i(wt)$ represents the current flowing through the device during the conduction period. T is the switching period. The forward voltage drop is calculated by using the following equation:

$$V_f = V_{f0} + r_f i(wt) \quad (3)$$

where V_{f0} and r_f show the forward voltage drop of the device at no load and the device forward resistance. The data sheet of the switching device provided by the manufacturer is used to calculate V_{f0} and r_f .

Substituting Eq. (3) into Eq. (2), results in Eq. (4):

$$P_{cond} = V_f I_{av} + I_{rms}^2 r_f \quad (4)$$

I_{av} is the average current flowing through the device while I_{rms} is the root mean square value of the current flowing through the device for the conduction period of the switching cycle [32]. These values of the current are calculated by using Eq. (5) and (6) respectively.

Fig. 9. Output voltage for single phase AC side cascaded topology with four H-bridges.

Fig. 10. Harmonic spectra of output voltage for single phase AC side cascaded topology with four H-bridges.

$$I_{av} = \frac{1}{T} \int_0^T i(wt) d(wt) \quad (5)$$

$$I_{rms}^2 = \frac{1}{T} \int_0^T i^2(wt) d(wt) \quad (6)$$

The combination of turning on losses and turning off losses results in the switching losses of the device. These losses depend on the device characteristics, switching frequency and the current, which is flowing through the device. The following relationship is used for the calculation of the switching losses of the device:

$$P_{sw} = \frac{f_s}{2\pi} \int_0^T ki(wt) dwt \quad (7)$$

where P_{sw} are the device switching losses, k is constant and is obtained from the switching energy graph of the device which is given in the data sheet. The switching frequency f_s has a direct impact on the switching losses. For the loss calculation, the current and voltage waveforms of

the switching devices must be known.

The present paper analyses the power losses in both the DC side and AC side cascaded converters for six different design cases (2 and 4H-bridge sub modules for the AC side cascaded topology and the DC side cascaded topology with 8 and 16 half bridge and full bridge sub modules) and compares their overall efficiency for a benchmark 500 MW power rating using the computer simulation based method. The nominal values of efficiency and losses quoted [46] for the existing East-West HVDC interconnector between Ireland and Wales are calculated and are used as a benchmark to verify the methodology used for power loss calculations presented in this paper.

As stated earlier, the East-West HVDC interconnector, the DC link voltage is 400 kV and the rated output power is 500 MW. If we consider a 9-level output voltage for the DC side cascaded topology, each arm will have 8 sub modules with 100 kV DC voltage across each sub module. With a 16 sub modules based design, each sub module voltage

Fig. 11. Output voltage for single phase DC side cascaded topology with 8 half-bridge sub modules.

Fig. 12. Harmonic spectra of output voltage for single phase DC side cascaded topology with 8 half-bridge sub modules.

will change to 50 kV, leading to a 17-level output voltage. The design for the AC side cascaded topology is different. Here, considering 2 full-bridges are cascaded on AC side of the two-level inverter, the DC link voltage for each full-bridge will be 100 kV [17]. If we consider, 4 full-bridges on AC side of two-level inverter, the DC link voltage will change to 50 kV. The characteristics of the converter switches are obtained from the datasheets of the 3.3 kV, 450 A, Infineon [47] and 1.7 kV, 800 A, ABB [48] switches. A safety coefficient of 1.15 has been applied to the device voltage ratings to ensure they can withstand the high DC link voltage for each converter. For example, for 100 kV, 35 Infineon 3.3 kV switches should be in series ($35 \times 3.3 \cong 115$) and for 50 kV, 34 ABB 1.7 kV switches should be series ($34 \times 1.7 \cong 57.5$). The number of parallel branches depends on the rated current of the system and the rated current of each switch.

The parameters of the AC side and DC side topologies used for the purpose of comparing converter losses are given in Tables 1 and 2. The comparison has been completed with the same input DC voltage and the same AC load. In the AC side cascaded topology, the proper output voltage with acceptable THD necessitates a 2 kHz switching frequency for level shifted carriers. Paper [17] introduces more details about the control and operation of the AC side cascaded topology.

For the DC side cascaded topology, phase shifted carrier pulse width modulation (PS-PWM) is considered as a superior method for control of sub modules because of its special features including even distribution

of stress and power between SMs and low total harmonic distortion (THD) of output voltage[35]. More details and operation principles are presented in [26].

Increasing the number of sub modules in DC side cascaded and AC side cascaded topologies, will lead to a lower voltage rating for the sub modules which implies switching losses may be lower because of using lower switch rating (1.7 kV, 800 A, ABB). Increasing the number of sub modules will not improve the efficiency of AC side cascaded topology (because at the same time losses for two-level inverter increases). However, the efficiency of DC side cascaded topology will be improved (because the sub module losses will be decreased). Fig. 3 shows the conduction losses and switching losses for the AC side cascaded topology with 2 and 4 sub modules on the AC side. The total loss calculation shows that increasing the number of sub modules will lead to higher losses and lower efficiency because of the increase in the two level inverter losses.

Fig. 4 depicts the conduction losses and the switching losses for the DC side cascaded topology at the same output power ($P_{out} = \frac{500}{3} MW$) with 8 and 16 half bridge sub modules. It can clearly be seen that the losses for the DC side cascaded with 16 sub modules decreases. The reason is that the voltage rating of the devices in the sub modules will be less. It should be noticed that the input DC voltage is the same for both topologies as well as output power.

The losses for the DC side cascaded topology with 8 and 16 full

Fig. 13. Output voltage for single phase DC side cascaded topology with 16 half-bridge sub modules.

bridge sub modules at the same output power has been shown in Fig. 5. The comparison of losses between two different topologies of the DC side cascaded structure (half bridge and full bridge sub modules) shows that the semiconductor losses will be increased understandably with full-bridge sub module structure (the number of devices in conduction path is twice of half-bridge sub module) and it is approximately twice of the half bridge sub module topology. Comparison of losses between the AC side cascaded topology and the full bridge sub module DC side cascaded structure confirms that both topologies have higher amount of losses rather than the half bridge sub module DC side cascaded topology.

Fig. 5 also depicts that the amount of losses will be decreased when we increase the number of full bridges from 8 to 16. Comparing the results of Figs. 4 and 5 it is understandable that the additional number of switches are contributing towards increase in losses for full bridge MMC. The only advantage of using full-bridge sub module is the feature of DC fault reverse blocking capability with cost of higher losses and higher number of devices.

With a choice of 3.3 kV, 450 A Infineon switch as a switching device, the existing two-level East-West inter-connector converter losses will be around 1.7% (the switching strategy is designed to eliminate the low order harmonics). The total loss for three phase will be around 9 MW and the efficiency will be 98.23%. So the total converter losses can be calculated as $100\% - 98.23\% \cong 1.7\%$. Therefore, based on the switching loss aspect comparison, and taking the commercial existing HVDC converter (East-West inter-connector) losses as reference (i.e. around 3 MW loss per phase, as shown in Fig. 6), if the half-bridge and full-bridge designs are considered, 16 sub modules half bridge configuration has the best performance index with a further loss reduction of $\frac{(3 - 1.11)}{3} * 100\% = 63\%$.

In terms of losses, 8 sub modules (SM) half bridge topology slightly reduces losses which is around 7.3%. The full bridge topology with 8 sub modules (SM) is not a suitable choice as it increases the losses by 50%. Next is 16 sub modules (SM) full bridge topology which can reduce the losses by 24%. Fig. 6 shows the details of the loss analysis for the six different case studies along with the benchmark (East-West Interconnector).

Fig. 14. Harmonic spectra of output voltage for single phase DC side cascaded topology with 16 half-bridge sub modules.

Table 3
Power and efficiency calculations for five case studies that can be applied for East-West inter-connection (500 MW, 400 kV).

Topology	Converter Losses (3 phase)	Efficiency	Advantages	Disadvantages	Standard Switch Type	Number of Levels	Voltage Rate on sub modules	THD Including Third Harmonic
Two-Level with 5th and 7th harmonic elimination (Existing East-West inter-connector)	9 MW	98.23%	(1) Simple control (2) Uses less amount of switches components (3) Good efficiency	(1) Needs AC filters on the AC side (2) Total system loss is relatively high (3) It doesn't have fault tolerant capability	Infineon 3.3 kV, 450A	Two-level	–	199.3%
AC side cascaded with 2 full-bridges on the AC side	6.39 MW	98.73%	(1) Higher DC voltage utilization because of floating capacitors (2) Has dc fault blocking capability (3) Small capacitor size	(1) It needs AC filters because of mis-match between two-level converter as high power stage and H-bridge cascaded sub modules	Infineon 3.3 kV, 450A	7-level with modulation index = 0.9	100 kV	63.11%
DC side cascaded with 8 half bridge sub-modules	8.4 MW	98.34%	(1) Good THD (2) Good efficiency (3) Doesn't need any AC filters	(1) Half-bridge DC side cascaded doesn't have fault tolerant capability (2) It needs a lot of components and voltage sensors (3) It has complicated control	Infineon 3.3 kV, 450A	9-level with modulation index = 0.9	100 kV	16.47%
DC side cascaded with 8 full bridge sub-modules	13.6 MW	97.35%	(1) Good THD (2) Good efficiency (3) Doesn't need any AC filters (4) Has DC fault blocking capability	(1) It needs a lot of components and voltage sensors (2) It has complicated control	Infineon 3.3 kV, 450A	9-level with modulation index = 0.9	100 kV	16.37%
AC side cascaded with 4 full-bridges on the AC side	9 MW	98.23%	(1) Higher DC voltage utilization because of floating capacitors (2) Has D fault blocking capability (3) Small capacitor size	(1) It needs AC filters because of synchronization mis-match between two-level converter as high power stage and H-bridge cascaded sub modules	Infineon 3.3 kV, 450A at two level stage and ABB 1.7 kV, 800 A for AC side sub modules	13-level with modulation index = 0.9	50 kV	57.5%
DC side cascaded with 16 half bridge sub-modules	3.36 MW	99.33%	(1) Good THD (2) Good efficiency (3) doesn't need any AC filters	(1) Half-bridge DC side cascaded doesn't have fault tolerant capability (2) It needs a lot of components and voltage sensors (3) It has complicated control	ABB 1.7 kV, 800 A	17-level with modulation index = 0.9	50 kV	7.52%
DC side cascaded with 16 full bridge sub-modules	6.81 MW	98.65%	(1) Good THD (2) Good efficiency (3) Doesn't need any AC filters (4) Has DC fault blocking capability	(1) It needs a lot of components and voltage sensors (2) It has complicated control	ABB 1.7 kV, 800 A	17-level with modulation index = 0.9	50 kV	7.55%

3.2. Comparison of the output voltage harmonic profile between DC side cascaded and AC side cascaded topologies

The harmonic content of the MMC output voltage and current are of particular importance and must be kept below permissible levels. This is typically done by increasing the switching frequency and/or by using an output filter stage. Some control techniques could decrease the harmonic content of the MMC output voltage in the DC side cascade and eliminate the need of any filter [36,37]. In the AC side cascaded topology, in order to reach the output voltage with a proper level of THD, the switching frequency of carriers has been considered as 2 kHz and the switching frequency of the main converter (two-level inverter) is 400 Hz. So, It requires a number of tuned filters to attenuate the 5th and 7th harmonics that may arise from synchronization mis-match of the two-level converter (main high power stage) and H-bridge cascaded sub modules (series active filter). Without such filters, the converter transformer will be exposed to excessive dv/dt . Figs. 7 and 8 show the output voltage and its harmonic spectra for the single phase AC side cascaded topology with two H-bridge sub modules on AC side. The parameters for simulation are according to Table 1 and the modulation index is 0.9.

Fig. 8 shows high amount of third harmonic order and THD. That is because of the third harmonic subtraction method which is proposed in [17] permits the hybrid cascaded multilevel converter to operate independent of load power factor over an extended modulation index

range and without any capacitor voltage balancing problems. From the application point of view, single phase AC side cascaded topology cannot be a proper choice because of its high amount of THD. However it can be a suitable option for the HVDC applications where in the three phase system, the third harmonic order is eliminated and THD is improved.

Figs. 9 and 10 show the output voltage and its harmonic spectra for single phase AC side cascaded topology with 4H-bridge sub modules on AC side. As seen from Fig. 10, the output voltage harmonic profile are slightly better than 2H-bridge topology.

For the DC side cascaded topology, the simulation parameters are according to Table 2 where the input DC voltage is 400 kV and 8 half bridge sub modules are cascaded in the each arm. Considering the modulation index of 0.9, Figs. 11 and 12 show the output voltage and its harmonic spectra.

Figs. 13 and 14 show the output voltage and its harmonic spectra with a modulation index 0.9 and 16 half bridge sub modules per arm.

The comparison between harmonic spectra of the output voltage for DC side cascaded topology and AC side cascaded topology shows that the DC side cascaded topology has a superior THD profile in the output which could make it a better choice for the single phase applications as well as HVDC applications. Another point is using the filters in the output of the AC side cascaded topology is essential to attenuate the 5th and 7th harmonics that may arise from synchronization mis-match between two-level and H-bridge cascaded sub modules.

Fig. 15. Short circuit current path during DC side fault for a half bridge sub module DC side cascaded topology before blocking the IGBT gate signals.

Fig. 16. Short circuit current path during DC side fault for AC side cascaded topology before blocking the IGBT gate signals.

Table 3 summarises the losses and efficiency calculations for the seven case studies.

3.3. Comparison of the DC fault current between half bridge sub module DC side cascaded and AC side cascaded topologies before blocking IGBTs occurs

For the future design of large multi-terminal HVDC networks, a detailed investigation into the behaviour of system under DC fault condition is vital. Various studies have been carried out on DC fault analysis with VSC configurations [38]. Recently, DC fault analysis of HVDC system based on modular multilevel converter (MMC) has attracted significant interest [39–43]. From the circuit configuration and operation points of view, the DC side cascaded topology has arm reactors in each converter arm whereas these are not present in the AC cascaded topology. However, both topologies have a large number of smaller distributed DC capacitors connected to each sub-module. In this section, the transient DC voltage and current after a DC side fault occurs will be studied. To analyse the behaviour of MMC during the DC short circuit usually two stages are considered. In stage one MMC remains operational until blocking of IGBT and due to the short period (a few milliseconds after a DC fault) the DC capacitors in the sub modules are considered constant [40]. In stage two all gate pulses are blocked and DC capacitors of the sub modules are isolated. In this stage; the AC sources inject currents through the freewheeling diodes [39].

In this paper, the analysis is conducted for the stage one which is

from the fault occurrence up to the time that the gate signals of IGBTs are withdrawn (or blocked). A typical short circuit current path for a half bridge sub module DC side cascaded MMC and AC side cascaded MMC are shown in Figs. 15 and 16. Cable parameters (L_C and R_C) are shown in Table 4.

The DC cable is represented by a simple RLC network. The capacitor C is because of the DC cable capacitance which is usually smaller than the capacitors used in the SMs. For a DC side cascaded structure, the total DC voltage in each converter leg equals the nominal DC link voltage which indicates that half of the SMs are connected to their internal DC capacitors. After occurrence of a DC fault, it usually takes few milliseconds to block the gate signals of the IGBTs. During this stage, the MMC remains operational and the DC cable capacitor will discharge as well as the capacitors within the SMs. However, due to the short discharge period of the SMs' DC capacitors their change is insignificant and their voltages will be considered as constant during this stage. According to short circuit current path, the simplified circuit during this stage for the half bridge sub module DC side cascaded topology is shown in Fig. 17 where V_{dc}^* is the nominal DC link voltage [40].

R_C , L_C and C are the DC cable parameters. Following the circuit analysis using Laplace transforms and considering initial conditions for L_{arm} , L_C and C results in the following expression for $i_{dc}(s)$:

Fig. 17. Simplified equivalent circuit for a half bridge sub module DC side cascaded topology before blocking the IGBT gate signals [40].

Table 4

System parameters during the DC short circuit.

Buffer inductance	L_{arm}	L_{arm}
Cable inductance	L_C	10 mH
Cable capacitance	C	100 μ F
Initial cable capacitance value	V_{C0}	400 kV
Nominal DC link voltage	V_{dc}^*	400 kV
Cable resistance	R_C	1 Ω
Initial current of buffer inductance	i_0	1245 A
Initial current for the line inductance	i_{cab0}	1245 A

Fig. 18. Simplified equivalent circuit for AC side cascaded topology before blocking the IGBT gate signals.

$$i_{dc}(s) = \frac{\frac{2L_{arm}L_cC}{3}s^3 + (\frac{2L_{arm}C}{3}R_c + CL_cV_{dc}^* - CL_cV_{C0})s^2 + (CR_cV_{dc}^* - CR_cV_{C0} + \frac{2L_{arm}}{3}i_0 + L_c i_{cab0})s + V_{dc}^*}{s(\frac{2L_{arm}}{3}CL_c s^3 + \frac{2L_{arm}}{3}CR_c s^2 + (\frac{2L_{arm}}{3} + L_c)s + R_c)} \quad (8)$$

where V_{C0} is initial DC link capacitor voltage, i_{cab0} initial current for the line inductance and i_0 is the initial current of buffer inductance before the DC fault which can be calculated by $\frac{V_{dc}}{R_{total}}$. So if we consider

$$V_{dc} = 400 \text{ kV and } P_{out} = 500 \text{ MW then } R_{Load} = \frac{V_{dc}^2}{P} = \frac{400^2}{500} = 320 \Omega.$$

The total resistor will be:

$$R_{total} = R_{Load} + R_c = 320 + 1 = 321 \Omega \text{ So } i_0 = \frac{400}{321} \cong 1245 \text{ A.}$$

Table 4, lists the system parameters used for DC fault analysis:

Substituting the above parameters in Eq. (9) and applying the inverse Laplace, the dc short circuit current will be:

$$i_{dc}(t) = (-806.7 + 6782i)e^{(-8.3-2450i)t}(-0.97 + 0.23i + e^{(4898i)t}) - 398,385e^{-83.35t} + 400,000 \quad (9)$$

In this paper, a simplified equivalent circuit has also been developed to evaluate the short circuit current path for the AC side cascaded topology and compared with the DC side cascaded topology which is presented in [40].

For the AC side cascaded topology, the simplified circuit is shown in Fig. 18 where V_{dc}^* is the nominal DC link voltage.

So according to equivalent circuit it can be seen:

$$V_{dc} = V_{dc}^* \quad (10)$$

Considering the initial conditions and using the Laplace transform $i_{dc}(s)$ will be:

$$i_{dc}(s) = \frac{V_{dc}^*}{s(R_c + L_c s)} + \frac{L_c i_{cab0}}{R_c + L_c s} + C(V_{dc}^* - V_{C0}) \quad (11)$$

Applying the inverse Laplace transform and substituting the parameters according to Table 4, $i_{dc}(t)$ gives:

$$i_{dc}(t) = 400000(1 - e^{-100t}) + 1245e^{-100t} \quad (12)$$

If we compare $i_{dc}(t)$ for both topologies, it can clearly be seen that the DC current after the fault grows exponentially and from an initial value to reach to the final value. However, for the DC side cascaded topology an oscillation can be observed on the DC fault current. This is due to the presence of the arm inductor. Simulation result for equivalent circuits of both topologies with the parameters given in Table 4, verify the accuracy of Eqs. (9) and (12). It has been assumed that the DC fault occurs at 0.2 sec.

There is a significant difference in the equivalent circuit of Figs. 17 and 18, representing topologies for DC side cascade and AC side cascade respectively. In Fig. 17, the DC side arm inductor (L_{arm} , as shown in Fig. 15) is in series with the nominal DC link of the HVDC system (V_{dc}^*), which is shown in the equivalent circuit of Fig. 17. In the equivalent circuit of AC side cascaded topology, L_{arm} is not present (Fig. 18). This is the reason, why there is initially a sharper rise of current in the AC side cascaded topology (Fig. 19) (highlighted in the small window). It is expected that the blocking of the switching devices will prevent the fault current from flowing into the circuits further for AC side cascaded and full bridge sub module DC side topologies, so stage two will not initiate.

Recent advances in HVDC circuit breakers show short interruption times of less than 5 ms can be achieved with novel topologies [44,45]. However, according to this study the magnitude of the DC short circuit current in the DC side cascaded topology has not significant difference with the magnitude of the DC short circuit in the AC side cascaded structure before blocking IGBT gate pulses.

Fig. 19. DC fault current for both topologies before blocking the IGBT gate signals.

4. Conclusion

A comparative study between the classic topologies of MMC which are the AC side cascaded and the DC side cascaded has been presented in this paper. Harmonic analysis of the output voltage, loss calculations and the DC fault current magnitude before the blocking the IGBT gate signals occurs are the aspects of the comparison considered in this paper. The results show that the output voltage THD of the DC side cascaded structure is superior to the AC cascaded topology. Moreover, the AC side topology requires a filter to eliminate the spikes that are appearing in the output because of the synchronisation problem between two-level inverter and H-bridges. From an efficiency and the loss point of view, increasing the number of sub modules will not improve the efficiency of the AC side cascaded topology. This makes it a poor choice for industry applications. However, in the DC side cascaded topology, increasing the number of sub modules, improves the THD and efficiency. It should be noted that increasing the number of sub modules increases the control complexity and investment costs. Hence the half bridge sub module DC side cascaded structure with 16 sub modules could be considered as an optimised topology as it has reasonable THD and losses as well control simplicity. The DC fault analysis before blocking IGBT gate pulses; shows that in the half bridge sub module DC side cascaded structure, the DC side fault contains an oscillation but its magnitude has not big difference with the DC side fault current of AC side cascaded topology. A simplified equivalent circuit has also been developed to evaluate the short circuit current path for the AC side cascaded topology as well as the DC side cascaded topology.

Appendix A. Supplementary material

Supplementary data to this article can be found online at <https://doi.org/10.1016/j.jepes.2019.05.019>.

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