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Operation of Three-level Single-Phase Half-Bridge NPC Inverter-Based Shunt Active Power Filter Under Non-Ideal Grid Voltage Condition With Sliding Mode Controller

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Abstract— In this paper, a new control method is presented for a single-phase three-level neutral point clamped half-bridge shunt active power filter with the aim of eliminating the grid current harmonics. It is shown that the proposed control method accurately detects the positive-sequence voltage component under distorted grid condition. With this feature, the performance of the single-phase active power filter under distorted grid voltage condition is improved considerably. Furthermore, the imbalance in the capacitor voltages which occurs in the half-bridge topology is eliminated by adding a feedback term to the current control loop. The performance of the proposed control method is verified by simulation results obtained from MATLAB/Simulink.

Index Terms—Distorted voltage, NPC inverter, sliding mode controller, shunt active power filter.

I. INTRODUCTION

With the rapid growth of the renewable energy sources and their integrations, the power grid has high penetration of the wind and solar energy. This raises the major concerns for the power quality due to the increased number of switching devices connected to the power grid [1]. The voltages and currents are polluted by the harmonic components generated from the power electronics devices and non-linear loads. One promising solution to improve the power quality in the power grid is to use a shunt active power filter (SAPF). The concept of using the SAPF has been proposed in 1970s. The main idea is to use a SAPF which is basically a power converter that generates harmonic currents to compensate the harmonic currents in the power grid. The SAPF has excellent compensation characteristics and is able to simultaneously suppress harmonic currents and also compensates for the reactive power. Two-level voltage source converters are widely used in the APF topologies. In the multi-level converters, the losses and switching frequency are lower than the conventional two-level inverters [2-4].

In this paper, a sliding mode control (SMC) approach is proposed for single-phase half-bridge SAPF operating under

non-ideal grid voltage condition. The proposed SMC utilizes the capacitor current and its derivative in the sliding surface function. Moreover, the proposed control method not only compensates the harmonic current and reactive power, but also balances the voltages across two capacitors in the dc-link.

This paper begins by introducing the single-phase half-bridge neutral-point-clamped (NPC) based active power filter and determination of reference current signal in Section II. Section III presents the compensation method to balance the voltage between two capacitors. Section IV explains in detail the synchronization method utilized to extract the sine function. Section V gives an insightful description of the SMC proposed in this paper and then Section VI shows the simulation results to verify the proposed method. Finally, Section VII delivers conclusions for the proposed control method simulated in the single-phase half bridge NPC-based active power filter.

II. SINGLE-PHASE HALF-BRIDGE NPC ACTIVE POWER FILTER MODEL

The configuration of SAPF is presented in Fig. 1. In this topology, a three-level NPC voltage source inverter is connected in parallel to the grid. The studied inverter has four switches and two diodes clamped to the point of two equal dc link capacitors, (C_{dc1} , C_{dc2}). The clamped diodes are used to produce zero voltage. In this topology, the ac side of the inverter is connected to the point of common coupling (PCC) with an inductor (L_c) and the midpoint of dc-link capacitors is directly connected to neutral. The current of inverter, $i_c(t)$ is measured by a current transducer (CT₂). The RC type load groups are supplied from the full-bridge diode rectifiers where the current on the load terminal is measured by another current transducer (CT₁).

It is well known that a non-linear load current in steady-state is usually a periodic signal with harmonic components as follows

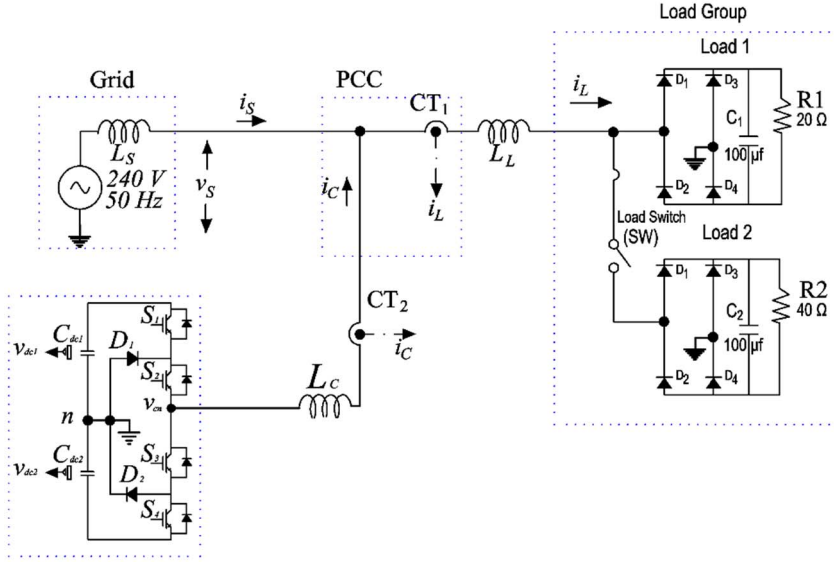


Fig. 1. Studied single-phase half-bridge APF.

$$\begin{aligned}
 i_L(t) &= \sum_{h=1}^{\infty} i_{L,h} \sin(h\omega t + \phi_h) \\
 &= i_{L,1} \sin(\omega t + \phi_1) + \sum_{h=2}^{\infty} i_{L,h} \sin(h\omega t + \phi_h)
 \end{aligned} \quad (1)$$

where ω is the angular frequency, h and ϕ_h are the harmonic order and harmonic phase angle, respectively. As presented in (1), the load current of the non-linear load groups consists of current at the fundamental frequency and harmonic currents defined as

$$i_L(t) = i_{L,1} + \sum_{h=2}^{\infty} i_{L,h} \quad (2)$$

Therefore, the harmonic currents should be controlled so as to inject a current which is equal to the harmonics, $i_{L,h}(t)$, with opposite phase, $i_c(t) = \sum_{h=2}^{\infty} i_{L,h} \sin(h\omega t + \phi_h)$. As well known, the control system is designed to regulate voltage(s) on the dc-link so that the grid current is forced to become sinusoidal by controlling the current between the PCC and inverter as follows

$$i_c(t) = \int \frac{v_s(t) - v_{cn}(t)}{L_c} dt \quad (3)$$

In order to obtain the compensation current reference, the amplitude of compensation current reference, I_s , should be determined and multiplied with a unity sine function as

$$i_s^*(t) = I_s \sin(\omega t) \quad (4)$$

However, it is important to note that the generation of unity sine function may be difficult when the grid voltage has

distortion. Under such circumstance, the pure sinusoid cannot be obtained correctly which causes degradation in the system performance [5]. As a consequence, it may not be possible to reduce the grid-current total harmonic distortion (THD) to less than 5%, as specified by the IEEE 519-1992 standard. Obtaining correct unity sine function will be discussed in Section IV.

On the other hand, the amplitude of the compensation current reference at the fundamental frequency is determined by using a proportional integral (PI) regulator as follows

$$\begin{aligned}
 I_s &= k_p(v_{dc}^* - [v_{dc1} + v_{dc2}]) \\
 &\quad + k_i \int (v_{dc}^* - [v_{dc1} + v_{dc2}]) dt
 \end{aligned} \quad (5)$$

where k_p and k_i are the proportional and integral gains of the PI regulator. The proper PI parameters can be obtained by trial and error method [6]. Voltage on the capacitors are equal to the half of the dc-link voltage, i.e., $v_{dc}/2$. Therefore, the capacitor voltages are added to determine total the dc link voltage, i.e., $(v_{dc} = v_{dc1} + v_{dc2})$. The PI regulator forces the dc link voltage, v_{dc} , to follow its reference, v_{dc}^* , during the power exchange between the grid and inverter. The main important issue is that v_{dc1} should be equal to v_{dc2} for the stability of the system, which will be explained in Section III in detail. The required compensation current reference, i_c^* , can be determined by subtracting the measured load current, i_L , from the grid current reference, i_s^* , i.e.,

$$i_c^* = i_s^* - i_L \quad (6)$$

Once the reference grid current waveform is determined, then the compensation current reference can be obtained correctly, as in (6). Then, the compensation current error can be obtained by subtracting the measured compensation current, i_c , from its reference, i_c^* [7]. The compensation current error, x_1 , is used to drive the switches (S_1 , S_2 , S_3 & S_4) of the inverter. The actual compensating current, i_c , which is

controlled by the SMC is explained in Section V. The switching pattern respect to the terminal voltage is presented in Table I. As can be seen in Table I, the switching pattern of NPC adds a zero voltage level at the output terminal of the inverter.

TABLE I
SWITCHING STATES

Output Voltage (v_{cn})	Pulses			
	S_1	S_2	S_3	S_4
$+v_{dc}$	1	1	0	0
0	0	1	1	0
$-v_{dc}$	1	0	0	1

III. COMPENSATION OF IMBALANCE IN CAPACITOR VOLTAGES

It is mentioned in Section II that there exists an imbalance in the capacitor voltages. One of the reasons of this imbalance comes from a dc offset caused by the system's initial condition. The other reason is the non-equal capacitance ($C_{dc1} \neq C_{dc2}$) values in practice [8], [9]. As clearly explained in [10], this imbalance in capacitor voltages can be eliminated if the imbalance variable ($v_{dc,e} = v_{dc1} - v_{dc2}$) is fed back and multiplied by a gain (k_e) which is added to $i_c^*(t)$ as follows

$$i_{c,e}^* = i_c^* + k_e v_{dc,e} \quad (7)$$

where $k_e < 0$. In this case, the compensating current track the modified references, $i_{c,e}^*$, instead of i_c^* .

IV. A SELF-TUNING GRID SYNCHRONIZATION METHOD AND GENERATION OF UNITY SINE FUNCTION

Fig. 2 shows the proposed structure which can be considered as a combination of a self-tuning filter and a conventional second-order generalized integrator (SOGI) and then named as SSOGI in [11]. It has the ability of providing two perfect orthogonal output signals, v' and qv' , under harmonic conditions of grid voltage v_s (v_α and v_β). The input signal is first passed through the self-tuning filter yielding a cleaner signal v_1 .

The SOGI block takes the signal v_1 and converts it into two in-quadrature outputs v' and qv' . These signals are then fed back to the self-tuning loop to correct v_1 . These operations are shown in Fig. 2. For the sake of simplicity, the SSOGI configuration can be separated into two subsystems: self-tuning and SOGI. The transfer functions of $v'(s)$ and $qv'(s)$ corresponding to input $v_1(s)$ in the s-domain can be recalled from [9] as follows

$$\begin{aligned} G_v(s) &= \frac{k_s \omega' s}{s^2 + k_s \omega' s + \omega'^2} \\ G_{qv}(s) &= \frac{k_s s^2}{s^2 + k_s \omega' s + \omega'^2} \\ G_{e_v}(s) &= \frac{s^2 + \omega'^2}{s^2 + k_s \omega' s + \omega'^2} \end{aligned} \quad (8)$$

where ω' is the center frequency [15] and k_s is a gain. The relationship between $v_1(s)$ and $v_s(s)$ can be written as

$$G_{v_1}(s) = \frac{k_s \omega' s}{s^2 + k_s \omega' s + \omega'^2} \quad (9)$$

Recall that $qv_1(s) = \frac{v(s)\omega'}{s}$, then

$$\begin{aligned} G_{v_1}(s) &= \frac{k_a(v_s(s) - v'(s)) - \omega'^2 v'(s)/s}{s} \\ &= \frac{k_a s v_s(s) - (k_a s + \omega'^2)v'(s)}{s^2} \end{aligned} \quad (10)$$

The transfer functions of the proposed SSOGI can be derived by substituting (8) into (6) as

$$\begin{aligned} G_{v_1}(s) &= \frac{k_a k_s \omega' s}{s^3 + k_s \omega' s^2 + (\omega'^2 + k_a k_s \omega')s + k_s \omega'^3} \\ G_{qv'}(s) &= \frac{k_a k_s \omega'^2}{s^3 + k_s \omega' s^2 + (\omega'^2 + k_a k_s \omega')s + k_s \omega'^3} \\ G_{e_v}(s) &= \frac{k_a k_s \omega'^2}{s^3 + k_s \omega' s^2 + (\omega'^2 + k_a k_s \omega')s + k_s \omega'^3} \end{aligned} \quad (11)$$

Compared to second-order system in conventional structure, the modified SSOGI is a third-order system which can perform better performance in removing the harmonic voltages. Further investigations into the SSOGI configuration behaviours are presented by the Bode plots of two transfer functions in Fig. 3(a). The output $qv'(s)$ behaves as a low-pass filter with -60 dB/dec attenuation while $v'(s)$ is a band-pass filter with a value of -40 dB/dec [16]. The system only supports the central frequency, ω' , and blocks all other high frequencies which are harmonic components. It is also obvious that the phase of $qv'(s)$ is shifted 90° below that of $v'(s)$. In other words, the two output signals are orthogonal in the steady-state.

The frequency controller in the DSOGI-FLL method is constructed by using the same technique presented in [12]. It detects the grid frequency based on e_v and qv' signals and provides this information back to the SOGI block. Similar to the frequency-lock loop in DSOGI-FLL [13], the frequency controller also identifies the grid frequency information based on the error signal e_v and output signal qv' .

The Bode plots of these signals, shown in Fig. 3(b), reveal that e_v and qv' are in phase if the input frequency is smaller than the SSOGI central frequency ($\omega < \omega'$) and are 180° difference or inversed in phase if ($\omega > \omega'$). From these characteristics, the frequency controller is also constructed as a first-order system [14]

$$\overline{\omega'} = -\Gamma(\overline{\omega'} - \omega) \quad (12)$$

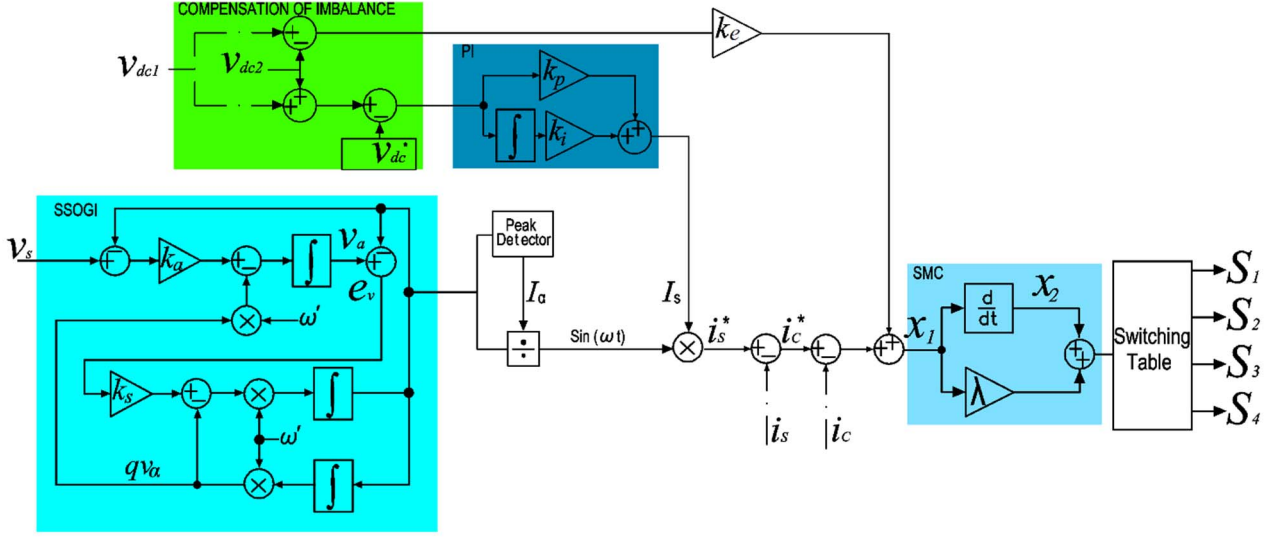


Fig. 2. Proposed control structure.

where $\bar{\omega}$ is the frequency at the operating point and ω' is the detected (real/practical) frequency and Γ denoted as the controller gain which is a function of input voltage magnitude and frequency.

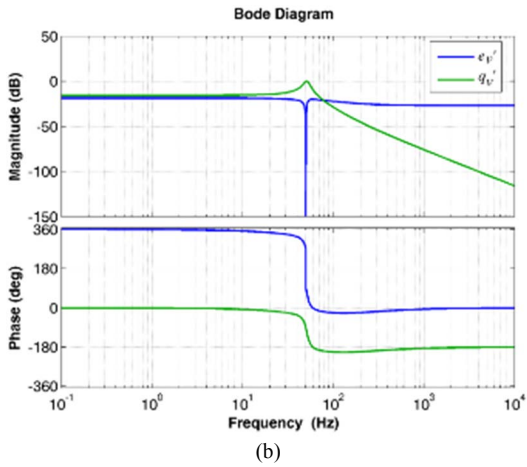
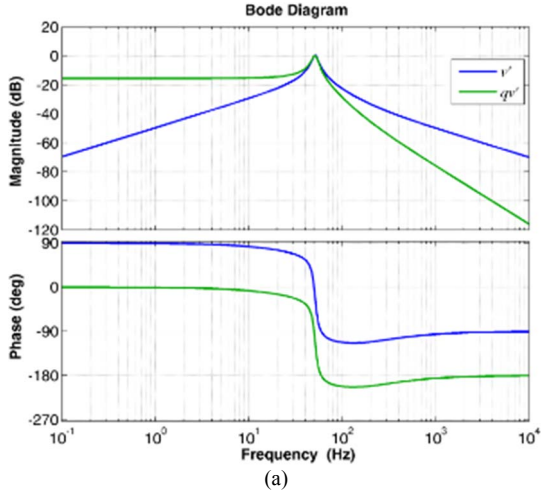


Fig. 3. Bode plots of (a) v' with qv' , and (b) e_v with qv' in the proposed SSOGI.

V. CURRENT CONTROLLER USING SMC

Let us define the compensation current error, x_1 , and its derivative as

$$x_1 = i_c - i_{c,e}^* \quad (13)$$

$$x_2 = \dot{x}_1 = \dot{i}_c - \dot{i}_{c,e}^* \quad (14)$$

where \dot{x}_1 denotes the derivative of x_1 , \dot{i}_c denotes the derivative of i_c . The sliding surface function is defined as

$$\sigma = \lambda x_1 + x_2 \quad (15)$$

where λ is a positive constant. When the system enters into the sliding mode ($\sigma = 0$), the state variables are forced to move on the sliding surface towards the origin ($x_1 = 0$ and $x_2 = 0$). In this case, the sliding mode is described by the following first-order equation

$$\dot{x}_1 = x_2 = -\lambda x_1 \quad (16)$$

Above equation represents a line passing through the origin with a slope equal to $-\lambda$. The movement of the state variables can be maintained on the sliding surface, if the following condition is satisfied

$$\sigma \dot{\sigma} < 0 \quad (17)$$

where $\dot{\sigma}$ denotes the time derivative of σ . The time derivative of (15) can be written as

$$\dot{\sigma} = \lambda \dot{x}_1 + \dot{x}_2 \quad (18)$$

The control input u is defined as

$$u = -\text{sign}(\sigma) \quad (19)$$

VI. SIMULATION RESULTS

The effectiveness of the proposed control method is verified by using MATLAB/Simulink along with the power system block set for performance verification purpose. In this study, the following system and control parameters are used.

Grid voltage parameters are: $v_s=240\text{V}$, $f=50\text{Hz}$, $L_s=1\text{ mH}$. Load parameters are: $R_1=20\Omega$, $C_1=100\mu\text{F}$, $R_2=40\Omega$, $C_2=100\mu\text{F}$, $L_L=6\text{mH}$. Inverter parameters are: $L_C=8.5\text{mH}$, C_{dc1} , $C_{dc2}=350\mu\text{F}$, $V_{dc}=680\text{V}$. The gains are selected as $k_e=-0.05$, $k_a=40$, $k_s=\sqrt{2}$ and $\Gamma=0.005$.

Two types of RC (Resistive and Capacitive) non-linear loads (Load 1 & Load 2) are used to observe the dynamic performances of the proposed system. The THD of the distorted grid voltage in the simulation study was computed to be 18.5%. Similarly, the THD of the load current for Load1 was computed as 29.96 %. Note that the rms value of load current in this case is 7A. When both loads (Load1 and Load2) are connected to the grid at the same time, the THD of the load current becomes 25.54 %. In this case, the rms value of the load current is 14A. The un-distorted grid voltage and load current waveforms for Load1 alone and Load1&Load2 together are shown in Fig. 4.

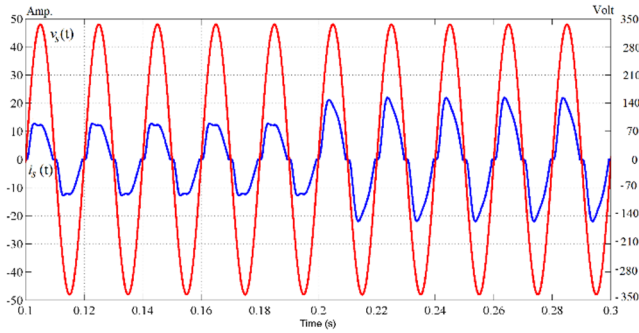


Fig. 4. Load current waveform under un-distorted grid voltage condition.

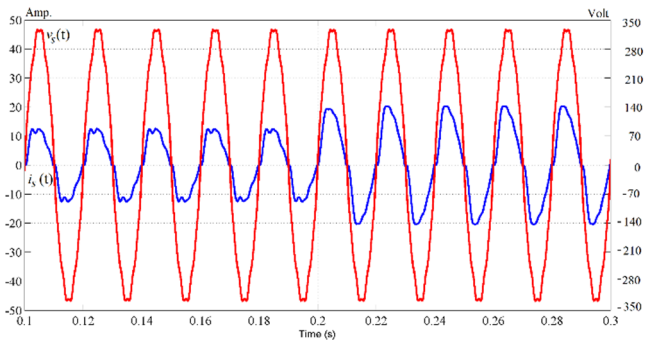


Fig. 5. Load current waveform under distorted grid voltage condition.

Fig. 5 shows the load current waveform under distorted grid voltage case. It can be seen that the grid voltage is not sinusoidal. Fig. 6 shows the grid current waveform under distorted grid voltage case obtained with the proposed control method. Comparing, Fig. 5 and Fig. 6, one can see that the grid current in Fig. 6 is sinusoidal and in phase with the grid voltage. The THD of the grid current has been computed to be 0.7 % which shows that the SAPF works

effectively to reduce the THD and achieve sinusoidal grid current.

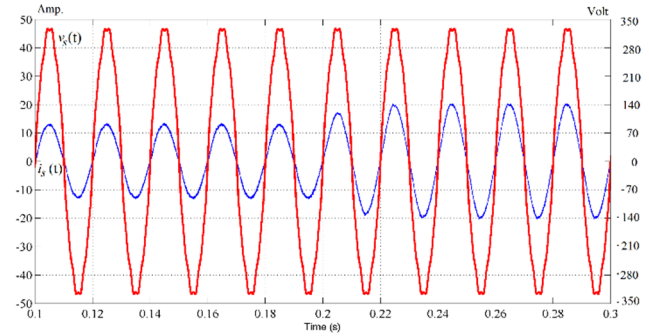


Fig. 6. Obtained grid current waveform under distorted grid voltage condition.

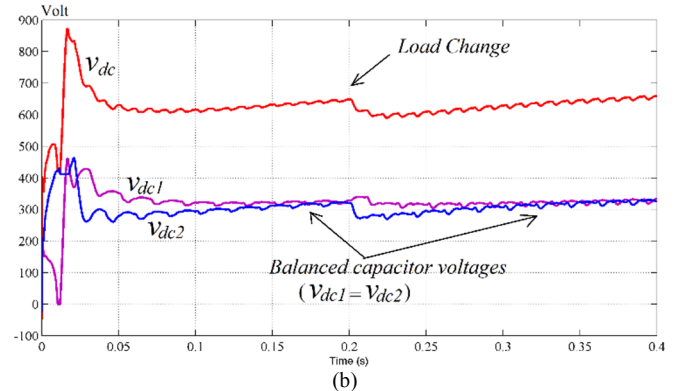
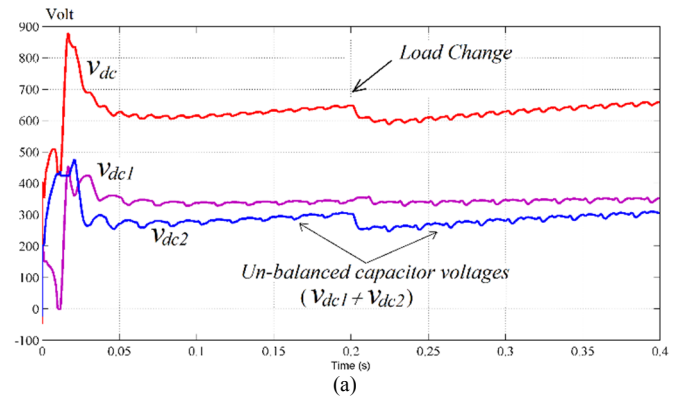


Fig. 7. Dc-link capacitor voltage waveforms: (a) without imbalance compensation loop, (b) with imbalance compensation loop.

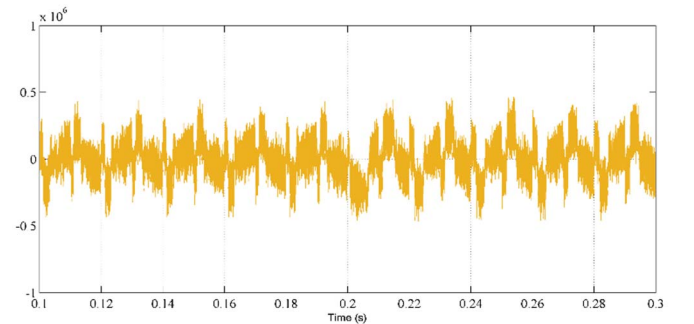


Fig. 8. Simulated dynamic response of σ .

Fig. 7 shows the capacitor voltages without imbalance and with imbalance compensation loops. As shown in Fig. 7(a), the dc-link capacitor voltages are not balanced when equation (7) is not used. However, when equation (7) is utilized, the dc-link capacitor voltages are balanced as shown in Fig. 7(b). Fig. 8 shows the simulated response of sliding surface function from which the control signals are generated using (19).

VII. CONCLUSION

In this study, a control method is proposed for a single-phase three-level neutral point clamped half-bridge shunt active power filter to eliminate the grid current harmonics under distorted grid voltage condition. It is shown that the positive-sequence component of the distorted grid voltage can be successfully obtained using SSOGI algorithm. The inverter current is controlled by using sliding mode control SMC strategy in which the sliding surface function is formed using the compensation current error and its derivative. In addition, an imbalance compensation loop is proposed which corrects the capacitor voltages effectively. Simulation results are presented and discussed to verify the validity of the proposed control approach.

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