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Full length article

Control strategy and hardware implementation for DC–DC boost power circuit based on proportional–integral compensator for high voltage application

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ABSTRACT

For high-voltage (HV) applications, the designers mostly prefer the classical DC–DC boost converter. However, it lacks due to the limitation of the output voltage by the gain transfer ratio, decreased efficiency and its requirement of two sensors for feedback signals, which creates complex control scheme with increased overall cost. Furthermore, the output voltage and efficiency are reduced due to the self-parasitic behavior of power circuit components. To overcome these drawbacks, this manuscript provides, the theoretical development and hardware implementation of DC–DC step-up (boost) power converter circuit for obtaining extra output-voltage high-performance. The proposed circuit substantially improves the high output-voltage by voltage-lift technology with a closed loop proportional–integral controller. This complete numerical model of the converter circuit including closed loop P-I controller is developed in simulation (Matlab/Simulink) software and the hardware prototype model is implemented with digital signal processor (DSP) TMS320F2812. A detailed performance analysis was carried out under both line and load regulation conditions. Numerical simulation and its verification results provided in this paper, prove the good agreement of the circuit with theoretical background.

1. Introduction

The classical DC–DC step-up (boost) power converter drastically suffers the restricted output-voltage due to the transfer gain ratio. Both output-voltage and efficiency are further reduced due to the self-parasitic behavior of the power circuit components. Moreover, two sensors (voltage and current) which are essential for control algorithm, increases the complexity and overall cost of the system when subjected to high-voltage applications [1–4]. Voltage-lift technology (i.e. additional passive (inductor/capacitor) components inclusion), implemented in power circuit design of electronic components is integrated to DC–DC power circuit system recently [1–8]. This provides an opportunity to design extra high-voltage (EHV) DC–DC power circuit, which actually derived from classical DC–DC buck power converter configuration [9–11].

Alternate solutions are also found in literatures to increase the output voltage, particularly on isolating the load side in order to ensure high-voltage operation of the DC–DC converter [12–14], while others were focused on [15–18].

- The boot-strap capacitors
- Power-conditioning circuits
- High-frequency transformers

The main drawback of these HV power converters are reduced efficiency and increased ripple in output waveforms. Although the isolated DC–DC power converters operate safely in HV applications, yet they are costlier and bulky in size due to inclusion of transformer. Furthermore, in case of utilization of the dynamically slow systems such as battery and fuel cell, the overall efficiency and the response of the system will be decreased in comparison to transformer-less configuration.

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The performance of the proposed EHV power circuit is advantageous in comparison to classical DC–DC configuration [1,2] as:

- Increased voltage transfer (k) gain ratio
- Wide range of control and reduced ripple components at the outputs
- Increased power density as well as efficiency
- Required closed loop P–I controller with one sufficient sensor (voltage feedback)

The numerical simulation software (Matlab/Simulink) model of the entire converter system based on governing equations is used for the operational modes of EHV power circuit unit and the analytical development of the entire system. The hardware

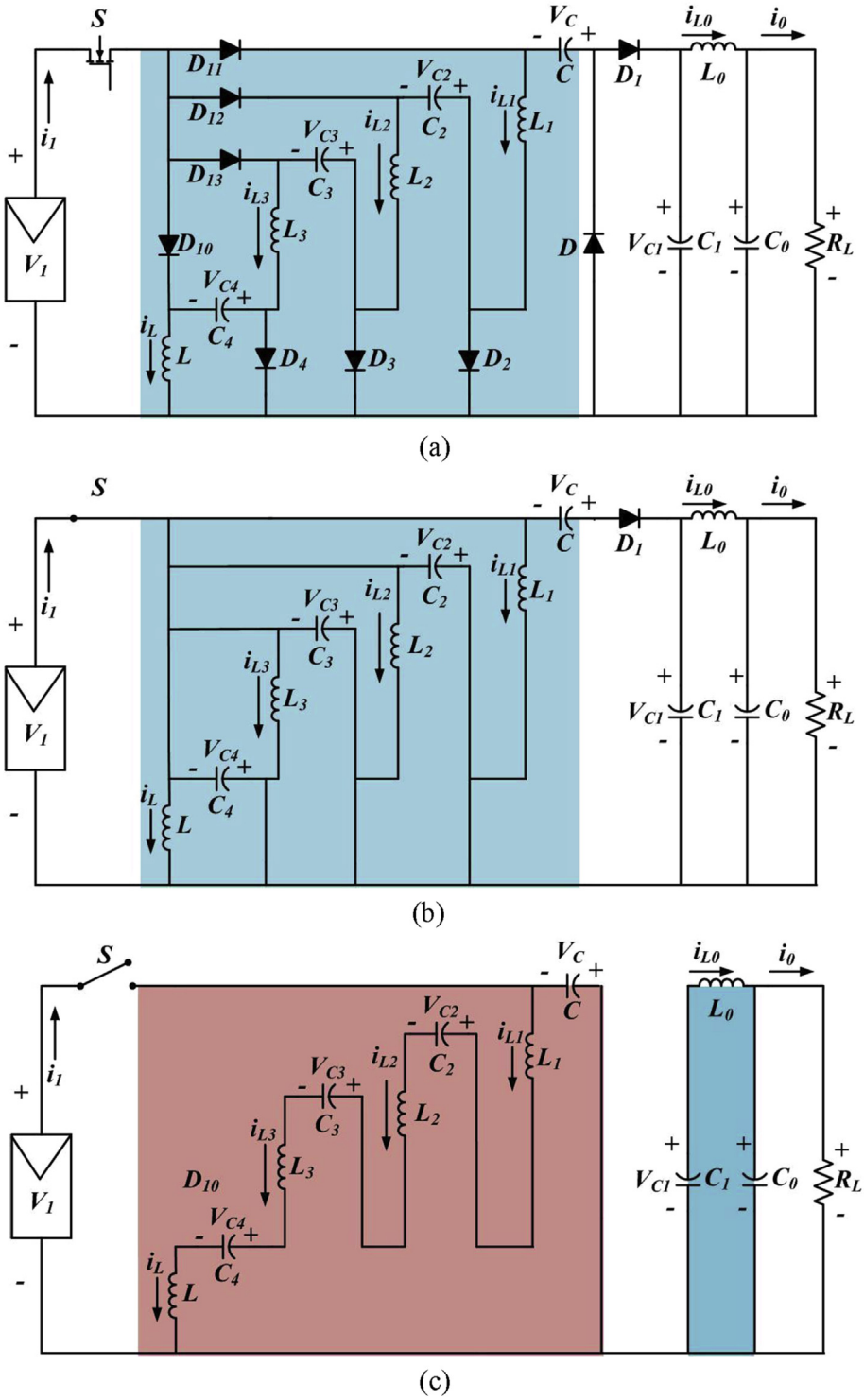

Fig. 1. (a) Investigated extra high voltage (HV) DC–DC boost power converter configuration; (b) Equivalent power converter circuit configuration during switch turned ON period; (c) Equivalent power converter circuit configuration during switch turned OFF period.

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prototype is implemented with complete controller algorithm written in TMS320F2812 processor. Analyses are carried out on both line and load variations to determine the performance of the whole EHV DC–DC converter system. Numerical simulations with experimental verification results provided in this paper matches closely with the analytical predictions.

2. EHV boost power converter configuration

EHV DC–DC boost power circuit diagram shown in Fig. 1(a), represents that the converter consists of N-channel MOSFET as static switch S, diodes (D, D_1, … , D_{13}), voltage-lift circuit with an inclusion of additional capacitors (C, C_1, … , C_4) and inductors (L, L_0, … , L_3). The voltage-lift gain is obtained by the capacitors (C_2, C_3 & C_4). The capacitor voltage (V_C) is built-up by the gain transfer ratio with the four times of the battery input voltage V_S ($V_{C0} = V_{C1}$). Fig. 1(a) indicates the voltage and current flow directions in the circuit. When the circuit operates in the continuous conduction mode, it is assumed that all components are ideal and capacitors are large enough. The load voltage (V_0), load current (I_0), supply voltage (V_1) and supply current (i_1) of the power circuit are depicted in the same Fig. 1(a) and its complete analytical predictions are provided in the next section.

3. Analysis of converter operating modes

Fig. 1(b) explains and provides the details about the instant at which the switch S is turned ON and its corresponding equivalent circuit. At this moment, the instantaneous input current (i_1-source current) gets equal to sum of all capacitor and inductor currents except i_{C0} and i_{C1}. The load current (I_0-load) flows through the circuit depending on the summation of the battery supply voltage V_1 and the capacitor voltage V_C. In this circumstance, the capacitors C_2, C_3 and C_4 are charged by the input voltage and increase all inductor currents.

Fig. 1(c) represents about the instant at which the switch S is turned OFF and its corresponding equivalent circuit. The instantaneous input current (i_1-source current) equals to zero at this interval. The inductors present in the voltage-lift part which is located on the left-hand side of capacitor C (L_1, L_2, L_3 and L) store the energy, while the capacitor C_2, C_3 and C_4 discharges the stored energy. Therefore, corresponding directions that are leading to charge the capacitor C are shown in the Fig. 1(c). At this situation, the current (i_{L0}) flows through the load over the inductor and decreases the current with all the inductors. In steady–state condition, the average inductor voltage will exist over a period as given below:

$$V_{C0} = V_0 \tag{1}$$

When switch $S$is turned ON, the circuit voltages appear as:

$$V_{C2} = V_{C3} = V_{C4} = V_1 \tag{2}$$

that also yields:

$$V_0 = V_{C1} = V_C + V_1 \tag{3}$$

It should be noted that, the inductor current I_L is increased during the period when the switch S is turned ON and is decreased during switch S is turned OFF. Therefore, the voltage components V_1 as well $-V_{L\text{-}OFF}$, which actually predicts the voltages across the inductor L as:

$$kTV_1 = (1 - k)\cdot TV_{L\text{-}OFF} \tag{4}$$

Table 1
Comparative performances emphasis the proposed DC–DC boost power converter with classical boost power converter.

Converter type	Output voltage (V_0) (Volts)	Output current (i_0) (Amps)
Classical converter	$V_0 = [k/(1-k)]\cdot V_1$	$i_0 = [(1-k)/k]\cdot i_1$
Proposed converter	$V_0 = [4/(1-k)]\cdot V_1$	$i_0 = [(1-k)/4]\cdot i_1$

$$V_{L\text{-}OFF} = [k/(1-k)]\cdot V_1 \tag{5}$$

Whereas, the voltages across inductors (L_1, L_2 and L_3) are determined as:

$$V_{L1\text{-}OFF} = [k/(1-k)]\cdot V_1 \tag{6}$$

$$V_{L2\text{-}OFF} = [k/(1-k)]\cdot V_1 \tag{7}$$

$$V_{L3\text{-}OFF} = [k/(1-k)]\cdot V_1 \tag{8}$$

The capacitor voltage V_C and output voltage V_0 are analytically predicted from Fig. 1(c) as:

$$V_C = V_{C\text{-}OFF} = V_{L\text{-}OFF} + V_{L1\text{-}OFF} + V_{L2\text{-}OFF} + V_{L3\text{-}OFF} + V_{C2} + V_{C3} + V_{C4} \tag{9}$$

$$V_C = 4k/(1-k)\cdot V_1 + 3V_1 \tag{10}$$

$$V_0 = V_C + V_1 \tag{11}$$

$$V_0 = [4/(1-k)]\cdot V_1 \tag{12}$$

Gain transfer ratio of output current and output voltage are predicted as:

$$i_0 = [(1-k)/4]\cdot i_1, \tag{13}$$

$$M_0 = 4/(1-k). \tag{14}$$

Finally, the average voltages and currents are described as:

$$V_C = [(3+k)/(1-k)]\cdot V_1, \tag{15}$$

$$V_{C1} = V_0, \tag{16}$$

$$V_{C2} = V_{C3} = V_{C4} = V_1. \tag{17}$$

$$i_{L0} = i_0, \tag{18}$$

$$i_L = [k/(1-k)]\cdot i_0, \tag{19}$$

Table 2
Comparative performances emphasis the simulation result of the proposed power circuit with classical power circuit unit (steady-state rated condition).

Duty ratio (k)	Output voltage (V_0) Classical converter	Output voltage (V_0) Proposed topology
0.1	1.11	44.44
0.2	2.5	50
0.3	4.28	57.14
0.4	6.66	66.66
0.5	10	80
0.6	15	100
2/3	19.999	120
0.7	23.33	133.33
0.8	40	200
0.9	90	400

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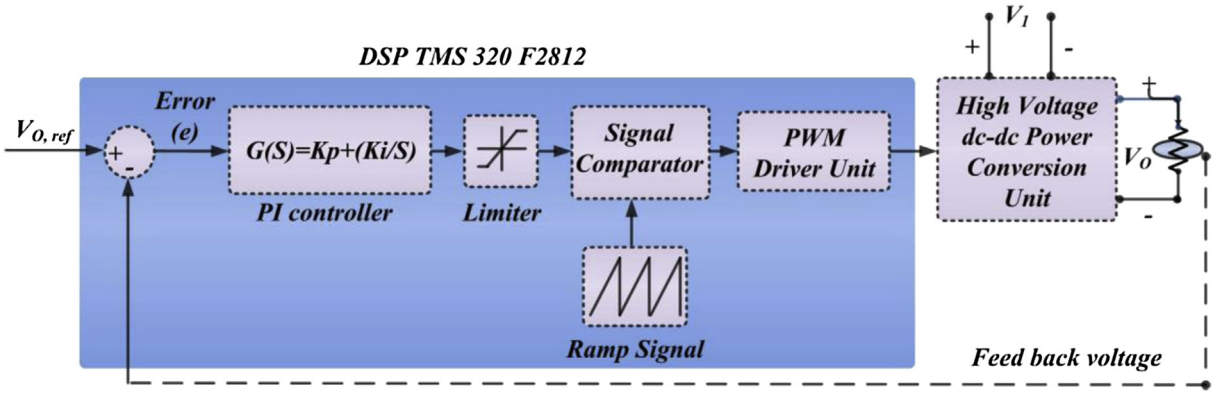

Fig. 2. Schematic circuit of simplified closed loop control strategy for power conversion unit under line/load regulation.

$$i_{L1} = i_{L2} = i_{L3} = i_L + i_{L0} = [1/(1-k)]i_0. \quad (20)$$

Table 1 explains the comparison between the EHV DC–DC boost proposed converter with the classical DC–DC boost converter with respected to voltage-life transfer gain k for better clarification. In addition, Table 2 proves the efficiency of the proposed power circuit in comparison with the classical DC–DC boost converter. It is noted that the classical one varies its output voltage from 1.11 V to 90 V with the set duty ratio k variation ranges from 0.1 to 0.9 and battery input voltage is 10 V respectively, while the proposed power circuit varies its output voltage from 44.44 V to 400 V.

Fig. 2 shows the closed loop P-I controller scheme for the power circuit and notably consists of one voltage sensor feedback without having any additional sensing unit for current. The feedback signal obtained from the DC load voltage is then compared with the set reference voltage $V_{dc.}$ Hence the obtained error between the set reference and feedback signal is applied to the P-I controller to compensate the available error. The manipulated signal provided by the P-I controller defines the set duty ratio k for pulse-width modulation (PWM) generator. The achieved set duty ratio k is then compared with the high frequency ramp-signal to provide controlled pulses for the static switch S. The controller parameters (P-proportional gain, I-integral gain) are fine-tuned to get the set reference DC voltage under different perturbation conditions. The P-I regulator transfer function are given by $G(s) = \frac{0.065011(s+9000)}{s}$ (simulation) and $G(s) = \frac{2.8(s+12000)}{s}$ (hardware), parameter are obtained based on bode plot technique and design concepts provided by [10,20].

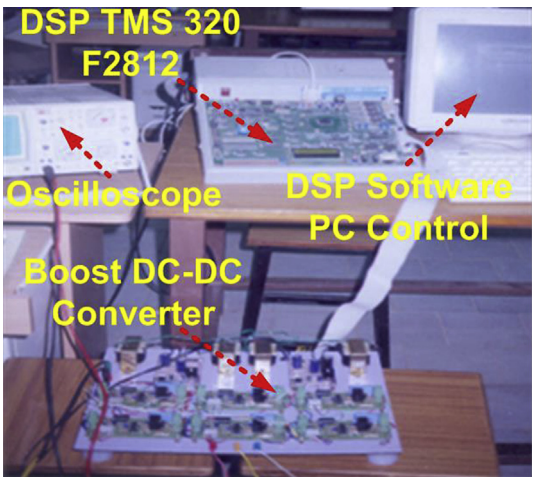

Fig. 3. Hardware prototype module of extra HV DC–DC boost power converter with DSP TMS320F2812 processor in closed loop operation.

Fig. 3 elaborates the hardware prototype model implementation based on TMS320F2812 processor with N-channel MOSFET (IRFPC60 version) EHV DC–DC power converter circuit. A set of numerical simulation as well as experimental results obtained are provided and discussed in detail in the next section.

4. Implementation and analysis of proposed DC–DC boost converter

a) Simulation and experimental results

Table 3, indicates the parameters taken into account for the numerical simulation test as well as experimental verifications. Inductance and capacitance values are determined with respect to the criteria of 5% (<2 mV) output ripple requirement as per IEEE standards [1,19].

Figs. 4 and 5 shows the simulated and experimental results at the rated condition of the set reference output voltage 120 V with the load resistance of 44Ω and duty ratio k = 2/3 (constant) of the proposed EHV DC–DC power converter. It is observed from the experimental result that the output voltage is slightly lower than the set reference and settles at 119.8 V with the negligible loss of 200 mV, which is caused by the self-parasitic effects of power circuit that is practically appreciable. This confirms that the output voltage closely matches (simulation/experimental) and verifies the prediction given by Eq. (12) at k = 2/3.

Correspondingly, Figs. 6 and 7 shows the output currents such as the simulated (2.7272 A) and experimental (2.722 A) observed. Obviously a small deviation is noticeable with the experimental result, as explained above due to the parasitic effects, which verifies the prediction given by Eq. (13) and satisfies the power-circuit laws.

Figs. 8 and 9 shows the output voltages where both the simulated (120 V) and experimental (119.8 V) results are obtained under same line and load perturbation condition. It is noticed that the output voltage stabilized at 0.005 s (simulated) and 0.625sec

Table 3
Parameters taken for simulation and hardware prototype for investigations.

Parameter		Value
Input voltage	(V_1)	10 V
Inductance	(L)	100 μH
Capacitance	(C)	5 μF
Load resistance	(R)	44 Ω
Duty ratio	(k)	2/3
Switching	(F_{SW})	50 KHz
Digital processor	DSP	TMS 320F2812
N-channel MOSFET	(IRFPC60)	$V_{DSS} = 600$ V, $R_{DS(ON)} = 0.40$ Ω, $I_D = 16$ A

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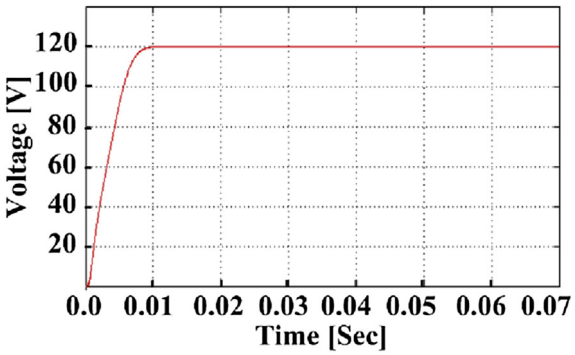

Fig. 4. Output voltage of extra HV DC–DC boost power converter with transient behavior (Simulation).

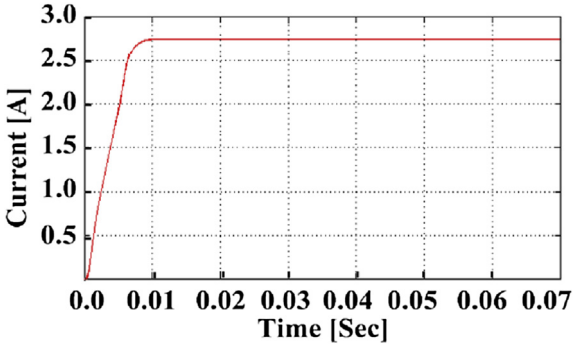

Fig. 5. Output current of extra HV DC–DC boost power converter with transient behavior (Simulation).

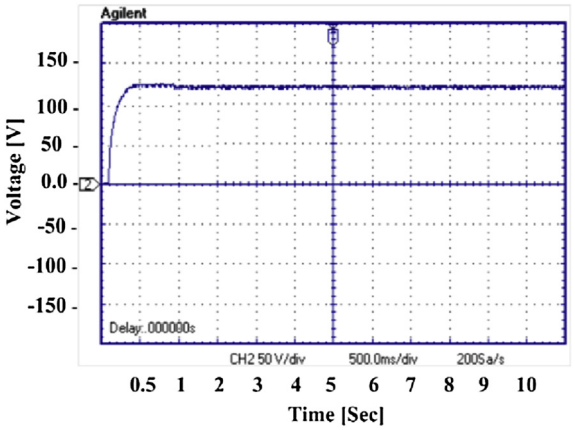

Fig. 6. Output voltage of extra HV DC–DC boost power converter with transient behavior (Experimental).

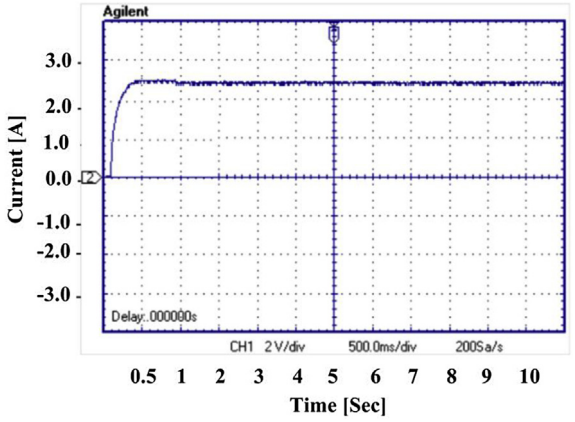

Fig. 7. Output current of extra HV DC–DC boost power converter with transient behavior (Experimental).

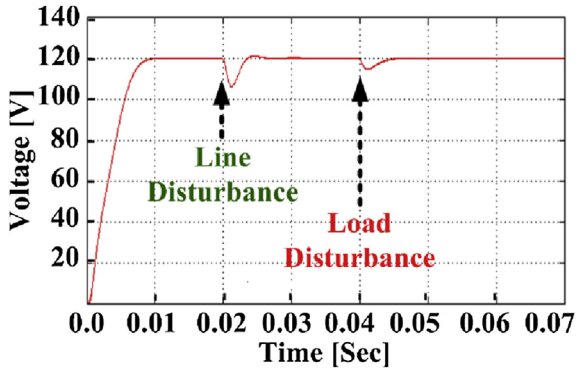

Fig. 8. Output voltage of extra HV DC–DC boost power converter with line-load regulation behavior (Simulation).

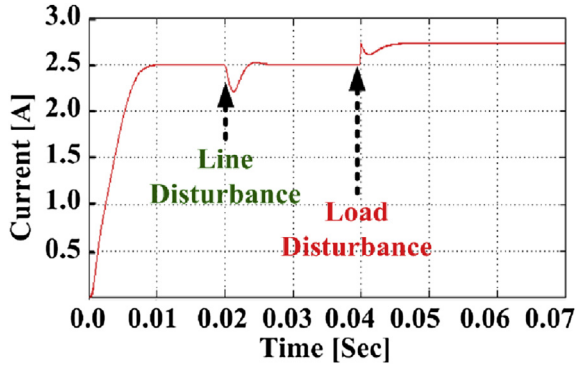

Fig. 9. Output current of extra HV DC–DC boost power converter with line-load regulation behavior (Simulation).

(experimental) by the closed-loop controller when the battery voltage represents a step variation from 10 V to 9 V.

Although the load resistance varies from 48 Ω to 44 Ω in the same analytical testing, the output voltage retains the same value of 120 V (set reference) in simulation and settles at 0.005 s, whereas the 119.8 V experimental result settles at 0.850 s as shown in Figs. 8 and 9 respectively. It is observable from experimental test, that the settling time required are little higher than simulated ones due to the parasitic effects. However, the output voltages of both the simulated and experimental results closely match and thereby verify the prediction given in Eq. (12).

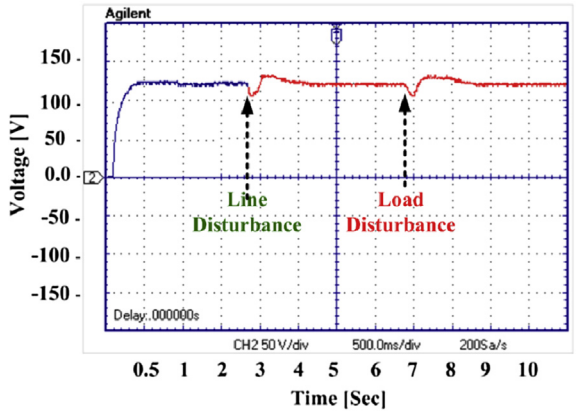

Fig. 10. Output voltage of extra HV DC–DC boost power converter with line-load regulation behavior (Experimental).

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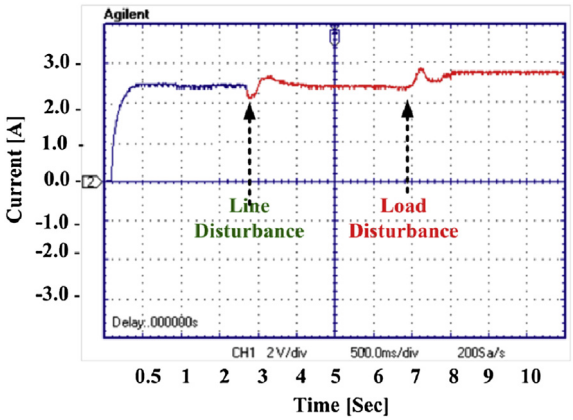

Fig. 11. Output current of extra HV DC–DC boost power converter with line-load regulation behavior (Experimental).

Figs. 10 and 11 correspondingly depict both the simulated and experimental output currents under the same line and load perturbation conditions. As expected both the simulated (2.5 A) and experimental (2.495 A) output currents remain the same value irrespective of variation in DC input voltage (battery) from 10 V to 9 V which settles at 0.005 s (simulated) and 0.625 s (experimental) respectively. Furthermore, if the load resistance is varied from 48 Ω to 44 Ω, load current increases from 2.5 A to 2.7272 A which gets settle at 0.005 s in the simulation, where as in the experimental study it increases from 2.495 A to 2.722 A and gets settle at 0.850 s. It is observed that the settling time slightly higher in case of experimental result due to self-parasitic nature and thereby it is practically appreciable. In addition, in this case both the simulated and experimental results closely match and thereby verify the prediction given in Eq. (13) by satisfying the power-circuit laws.

Further, a complete set of performance outputs obtained from numerical simulation and experimental tests are summarized in Table 4. All operating conditions (duty cycle variation $k = 0.1–0.9$) the converter performed with efficiency of 100% in simulation and 99% in experimental test with reduced ripple content of 0.22% in simulation and 0.43% in experimental test at the outputs is observed. Finally, the both simulation and experimental test parameters, the output voltage (V_O), output current (i_O) and efficiency (η) from the Table 4 are shown in three-dimensional (radar plot) view given by Fig. 12, to confirms the results (simulation/experimental) obtained are very closely matched.

Complete investigation test confirms that the proposed converter produce high efficiency, due to the fact that inclusion of additional passive (L, C) components. This actually reduces the several parasitic effects (L, R, C, and MOSFET switching, conduction etc.) [21], i.e. losses and increases the voltage transfer ratio gain k, which is actually proved in Eq. (12). It is verified by the generated outputs of hardware prototype having losses in the range of milli-amplitude which is practically appreciable. Also, DSP has its own sampling rate to interface with external hardware modules in real time, still the outputs settles less than 1 s in all investigated test.

b) Power Loss Analysis of Proposed DC–DC Converter

In literatures, the parasitic effects due to inductance are neglected in investigations of DC–DC converters. Hence, the RC time constant of converter is always comparable to the switching frequency to attain high efficiency. Therefore, the small parasitic inductance is considered, the results could differ and the inductance connected in the circuit, the current can be expressed by the following equation [21]:

$$i(t) = \frac{V_O}{R} e^{-\frac{t}{RC}} + I_{Load} \tag{21}$$

where, V_O is the initial voltage difference between the voltage source and the voltage across the capacitor. By considering the parasitic inductor, the input current is given by:

Table 4
Investigated output performance indices of numerical simulation and hardware prototype testing.

Duty ratio (k)	Output voltage (V_O) volt	Output current (i_O) amp	Output power (P_O) watt	Input voltage (V_I) volt	Input current (i_I) amp	Input power (P_I) watt	% Efficiency (η)	% Ripple
Simulation study performances								
0.1	44.44444	1.010101	44.89338	10	4.489338	44.89338	100	0.238
0.2	50	1.136364	56.81818	10	5.681818	56.81818	100	0.235
0.3	57.14286	1.298701	74.2115	10	7.42115	74.2115	100	0.233
0.4	66.66667	1.515152	101.0101	10	10.10101	101.0101	100	0.22
0.5	80	1.818182	145.4545	10	14.54545	145.4545	100	0.22
0.6	100	2.272727	227.2727	10	22.72727	227.2727	100	0.22
2/3	**120**	**2.7272**	**327.264**	**10**	**32.7264**	**327.264**	**100**	**0.22**
0.7	133.3333	3.030303	404.0404	10	40.40404	404.0404	100	0.22
0.8	200	4.545455	909.0909	10	90.90909	909.0909	100	0.22
0.9	400	9.090909	3636.364	10	363.6364	3636.364	100	0.22
Experimental study performances								
0.1	44.24444	1.004901	44.46129	10	4.466227	44.66227	99.55	0.486
0.2	49.8	1.131164	56.33195	10	5.655818	56.55818	99.6	0.478
0.3	56.94286	1.293501	73.65566	10	7.391436	73.91436	99.65	0.472
0.4	66.46667	1.509952	100.3614	10	10.06634	100.6634	99.7	0.466
0.5	79.8	1.812982	144.6759	10	14.50385	145.0385	99.75	0.441
0.6	99.8	2.267527	226.2992	10	22.67527	226.7527	99.8	0.432
2/3	**119.8**	**2.722**	**326.094**	**10**	**32.664**	**326.64**	**99.83**	**0.431**
0.7	133.1333	3.025103	402.7421	10	40.33471	403.3471	99.85	0.431
0.8	199.8	4.540255	907.1429	10	90.80509	908.0509	99.9	0.431
0.9	399.8	9.085709	3632.466	10	363.4284	3634.284	99.95	0.431

Bold values represent parameter taken for experimental and simulation task in closed operation.

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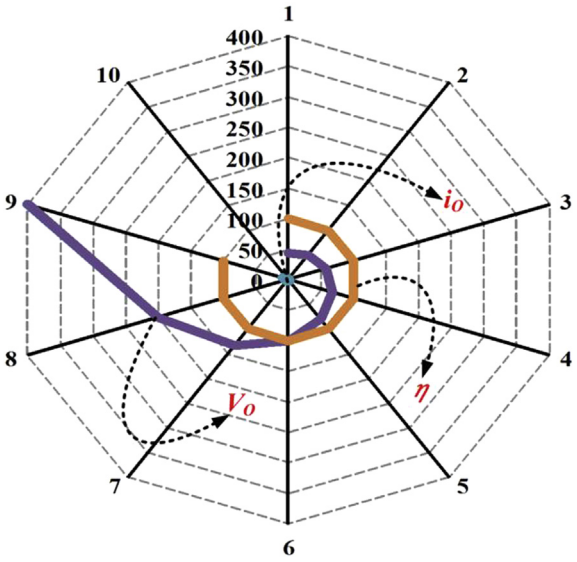

Fig. 12. Output performances of simulation and experimental test in 3D (radar plot) response. [*X*-axis: Output voltage (V_O) (50 v/div), *Y*-axis: Output current (i_O) (50 amp/div), *Z*-axis: Efficiency (η) (50 amp/div)].

$$i(t) = I_{Load}e^{-\frac{R}{2L}t}\cos\left(\sqrt{\frac{1}{LC}+\left(\frac{R}{2L}\right)^2}t\right) + I_{Load} + \frac{V_O - \frac{RI_O}{2}}{\sqrt{\frac{L}{C}-\left(\frac{R}{2}\right)^2}}e^{-\frac{R}{2L}t}\sin\left(\sqrt{\frac{1}{LC}+\left(\frac{R}{2L}\right)^2}t\right) \quad (22)$$

Further,

$$i(t) = I_{Load} + f(I_O, V_O)e^{-\frac{R}{2L}t} \times \sin\left(\sqrt{\frac{1}{LC}+\left(\frac{R}{2L}\right)^2}t + \varphi(I_O, V_O)\right) \quad (23)$$

where, $I_{Load} + I_O$ and V_O are the initial current and initial voltage difference between the input voltage and capacitor. The conduction loss of the circuit is directly proportional to the square of the rms value. Based on the above equations, one can easily numerically calculate the ratio of rms current over the average current based on the different parameters, and from which the loss can be calculated. The conduction losses of the MOSFET can be calculated by:

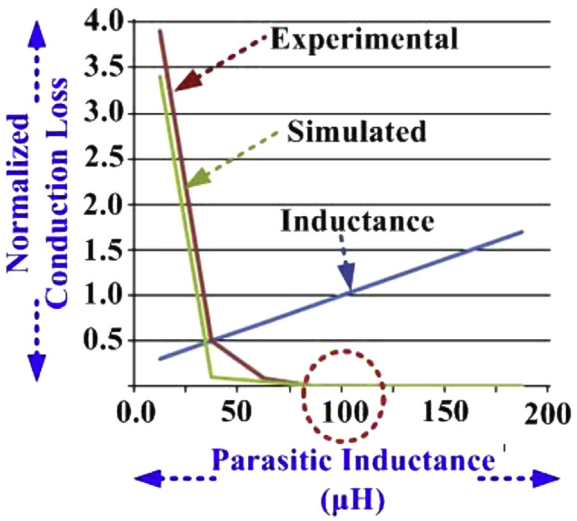

Fig. 13. Normalized conduction loss versus inductance variation.

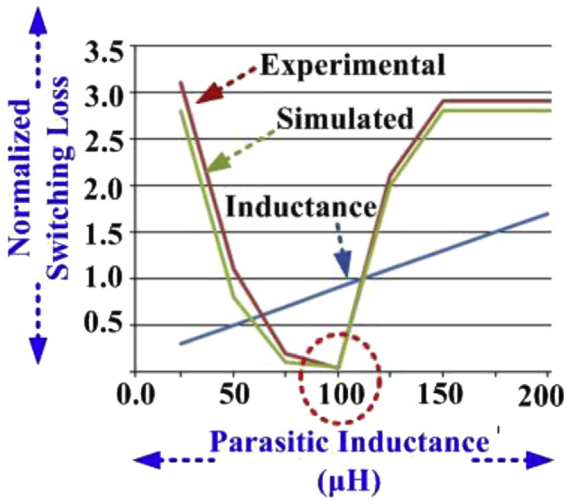

Fig. 14. Normalized switching loss versus inductance variation.

$$P_{COND.} = I_{ON}^2 R_{DS,ON} \quad (24)$$

where, I_{ON} is the drain current of the MOSFET, when it is ON state, $R_{DS,ON}$ is the drain-source resistance of the MOSFET, when it is ON state. Therefore, to obtain the average value of the conduction loss, the above Eq. (24) simply multiply by the duty ratio (k) of the MOSFET.

The switching losses of the MOSFET are due to the non-zero product of the drain current (I_D) and drain to source voltage (V_{DSS}). If the MOSFET were an ideal switch, the rise- and fall time of the current and voltage would be zero and would not have any switching loss. Then, switching losses can be calculated by:

$$P_{SW} = \frac{T_{SW,ON}V_{OFF}I_{ON}F_{SW}}{2} + \frac{T_{SW,OFF}V_{OFF}I_{ON}F_{SW}}{2} \quad (25)$$

where, V_{OFF} is the drain source voltage of the MOSFET, when it is OFF state, $T_{SW,ON}$, $T_{SW,OFF}$ are the time to turn the MOSFET ON and OFF state, and F_{SW} is the switching frequency. From Table 3, N-channel MOSFET ON state resistance R_{DS} (0.4Ω), C each capacitor (5 μF), L each inductor (100 μH), and F_s switching frequency (50 kHz) with duty ratio $k = 2/3$ (i.e. $T_{SW,ON} = 2/3*1/50$ KHz, $T_{SW,ON} = 1/3*1/50$ KHz) set for calculate the losses by Eqs. (24) and (25).

Figs. 13 and 14 depicts the variation of normalized conduction and switching loss when parasitic L changes (simulation/experimental). It is observed, that the conduction losses are dramatically reduced with variation of inductance profile (at 100 μH). Relatively, the switching loss is reduced and minimal at the resonant point (at 100 μH) and further increased with variation of inductance profile. It is concluded that, the increasing parasitic effects of power converters can be overcome by inclusion of additional passive components (L and C i.e. voltage lift technique) within the power circuit without any additional external compensation network/circuitry [1–9,21].

Finally, the obtained performances higher output voltage and higher efficiency, reduced % ripple and faster settling time (Table 4), which verifies that the proposed DC–DC converter (hardware

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prototype) has better power density factor as per standard [22–24]. Proving exact viability for parasitic compensation and suits the high voltage industrial needs.

5. Conclusion

Experimental implementation of hardware prototype EHV DC–DC boost power converter based on DSP TMS320F2812 process controller is described along with the relevant theoretical validations in this manuscript. The DC–DC power converter circuit integrated with the voltage-lift technology generates a high performance output-voltage compared to the conventional DC–DC boost converter whereas the duty ratio remains the same. This approach significantly overcomes the parasitic effects and reduces ripples at the output waveforms (voltage/current). A close loop controller with only one voltage sensor feedback, algorithm is developed to maintain the output voltage requirements under the line and load perturbation conditions. Simulation results provided in this manuscript are in accordance with the experimental results that are verified by the theoretical predictions. Hence the analyzed EHV DC–DC converter is suitable for the industrial applications, where the high-voltage becomes mandatory with reduced ripple at the output.

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References

[1] P. Sanjeevikumar, K. Rajambal, Extra high voltage DC–DC boost converters with simplified control strategy, Int. J. Modeling and Simulation 2008 (2008) 8. Hindawi Publishing Corporation, US, Article ID 593042.
[2] P. Sanjeevikumar, B. Geethalakshmi, DC–DC buck converter operated in boost mode for high voltage applications, in: Proc. National Level Power Engineering Conference (MEPPCON'06), MEPPCO Schlenek Engineering College, India, 2006, pp. 195–199.
[3] K. Ramash Kumar, S. Jeevananthan, Design and implementation of reduced order sliding mode controller plus proportional double integral controller for negative output elementary super lift Luo-converter, Trans. IET Power Electronics 6 (5) (2013) 974–989.
[4] K. Ramash Kumar, S. Jeevananthan, Modelling and implementation of fixed switching frequency sliding mode controller for negative output elementary super lift Luo-converter, Trans. IET Power Electronics 5 (8) (2012) 1593–1604.
[5] K. Ramash Kumar, S. Jeevananthan, Analysis, design and implementation of hysteresis modulation sliding mode controller for negative output elementary boost converter, Int. J. Electric Power Comp. Systems (IJEPCS) 40 (2) (2012) 292–311. Taylor & Francis Publications.
[6] Y. He, F.L. Luo, Analysis of Luo converter with voltage lift technique, Proc. IEE Conf Power Appl. 152 (5) (Sept. 2005).
[7] F.L. Luo, Y. Hong, Positive output super-lift converters, Trans. IEEE Power Electronics 18 (1) (January 2003) 105–113.
[8] Luo, F.L., Chen, X.F. "Self-Lift DC-DC Converters", Proc. IEEE Power Electronics drives and Energy Systems for Industrial Growth (IEEE-PEDES'98), vol. 1, pp.441–446, 1–3 December 1998.
[9] Luo, F.L. "Luo-Converters, A Series of New DC-DC Step-up (Boost) Circuit" Proc. IEEE Power Electronics and drives Systems (IEEE-PEDS'97), Singapore, pp. 582–588, 26–29 May, 1997.
[10] Katsuhiko Ogata, Modern Control Engineering, 2nd ed., Prentice-Hall of India Private Limited, New Delhi, 1996.
[11] K.M. Medley, S. Cuk, Dynamics of one cycle controlled Cuk converter, Trans. IEEE Power Electronics 10 (6) (1995) 634–639.
[12] K.-I. Hwu, T.-J. Peng, High-voltage-boosting converter with charge pump capacitor and coupling inductor combined with buck-boost converter, Trans. IET Power Electronics 7 (1) (January 2014) 177–188.
[13] Changwoo Yoon, Joongeun Kim, Sewan Choi, Multiphase DC–DC converters using a boost-half-bridge cell for high-voltage and high-power applications, Trans. IEEE Power Electronics 26 (2) (February 2011) 381–388.
[14] M. Nymand, M.A.E. Andersen, High-efficiency isolated boost DC–DC converter for high-power low-voltage fuel-cell applications, Trans. IEEE Industrial Electronics, 57 (2) (February 2010) 505–514.
[15] C.S. Leu, Pin-Yu Huang, Ming-Hui Li, A novel dual-inductor boost converter with ripple cancellation for high-voltage-gain applications, Trans. IEEE Industrial Electronics 58 (4) (April 2011) 1268–1273.
[16] L.H.S.C. Barreto, P. Peixoto Praca, D.S. Oliveira, R.N.A.L. Silva, High-voltage gain boost converter based on three-state commutation cell for battery charging using PV panels in a single circuit stage, Trans. IEEE Power Electronics 29 (1) (January 2014) 150–158.
[17] C.S. Leu, Ming-Hui Li, A novel current-fed boost converter with ripple reduction for high-voltage circuit applications, Trans. IEEE Industrial Electronics 57 (6) (June 2010) 2018–2023.
[18] K.I. Hwu, C.F. Chuang, W.C. Tu, High voltage-boosting converters based on bootstrap capacitors and boost inductors, Trans. IEEE Industrial Electronics 60 (6) (June 2013) 2178–2193.
[19] M.H. Rashid, Power Electronics Circuits, Devices and Applications, second ed., Prentice-Hall, USA, 1993.
[20] Darko Ostoji, A Multilevel Converter Structure for Grid-Connected PV Plants [Ph.D. theses], in: XXII Cycle, University of Bologna, Italy, March 2010. Available online: http://www.die.ing.unibo.it/dottorato_it/Ostojic/Tesi_Ostojic.pdf.
[21] Miaosen Shen, Fang Zheng Peng, Leon M. Tolbert, Multilevel DC–DC power conversion system with multiple DC sources, Trans. IEEE Power Electronics, 23 (1) (2008) 420–426.
[22] Johann Kolar, Uwe Drofenik, Juergen Biel, Marcelo Heldwein, Hans Ertl, Thomas Friedli, et al., PWM converter power density barriers, IEE J. Trans. Ind. Appl. 128 (4) (2008) 1–14.
[23] A. Matthew Porter, An Investigation of DC–DC Converter Power Density Using Si and SiC MOSFETS, U.S.N.A., Trident Scholar Project Report, no. 391, United States Naval Academy, Annapolis, Maryland, 2010.
[24] Jeff Ham. "Thermal considerations: assuring performance of Vicor's maxi, mini, micro series high-density DC–DC converter modules", The Power Bench, Published by Vicor Corporation, Andover, MA 01810, pp. 1–3.

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