Control Strategy And Hardware Implementation For DC–DC Boost Power Circuit Based On Proportional–Integral Compensator For High Voltage Application

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Full length article

Control strategy and hardware implementation for DC–DC boost power circuit based on proportional–integral compensator for high voltage application

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A B S T R A C T

For high-voltage (HV) applications, the designers mostly prefer the classical DC–DC boost converter. However, it lacks due to the limitation of the output voltage by the gain transfer ratio, decreased efficiency and its requirement of two sensors for feedback signals, which creates complex control scheme with increased overall cost. Furthermore, the output voltage and efficiency are reduced due to the self-parasitic behavior of power circuit components. To overcome these drawbacks, this manuscript provides, the theoretical development and hardware implementation of DC–DC step-up (boost) power converter circuit for obtaining extra output-voltage high-performance. The proposed circuit substantially improves the high output-voltage by voltage-lift technology with a closed loop proportional–integral controller. This complete numerical model of the converter circuit including closed loop P-I controller is developed in simulation (Matlab/Simulink) software and the hardware prototype model is implemented with digital signal processor (DSP) TMS320F2812. A detailed performance analysis was carried out under both line and load regulation conditions. Numerical simulation and its verification results provided in this paper, prove the good agreement of the circuit with theoretical background.

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1. Introduction

The classical DC–DC step-up (boost) power converter drastically suffers the restricted output-voltage due to the transfer gain ratio. Both output-voltage and efficiency are further reduced due to the self-parasitic behavior of the power circuit components. Moreover, two sensors (voltage and current) which are essential for control algorithm, increases the complexity and overall cost of the system when subjected to high-voltage applications [1–4]. Voltage-lift technology (i.e. additional passive (inductor/capacitor) components inclusion), implemented in power circuit design of electronic components is integrated to DC–DC power circuit system recently [1–8]. This provides an opportunity to design extra high-voltage (EHV) DC–DC power circuit, which actually derived from classical DC–DC buck power converter configuration [9–11].

Alternate solutions are also found in literatures to increase the output voltage, particularly on isolating the load side in order to ensure high-voltage operation of the DC–DC converter [12–14], while others were focused on [15–18].

- The boot-strap capacitors
- Power-conditioning circuits
- High-frequency transformers

The main drawback of these HV power converters are reduced efficiency and increased ripple in output waveforms. Although the isolated DC–DC power converters operate safely in HV applications, yet they are costlier and bulky in size due to inclusion of transformer. Furthermore, in case of utilization of the dynamically slow systems such as battery and fuel cell, the overall efficiency and the response of the system will be decreased in comparison to transformer-less configuration.

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The performance of the proposed EHV power circuit is advantageous in comparison to classical DC–DC configuration [1,2] as:

- Increased voltage transfer (k) gain ratio
- Wide range of control and reduced ripple components at the outputs
- Increased power density as well as efficiency
- Required closed loop P–I controller with one sufficient sensor (voltage feedback)

The numerical simulation software (Matlab/Simulink) model of the entire converter system based on governing equations is used for the operational modes of EHV power circuit unit and the analytical development of the entire system. The hardware

![Diagram](image)

**Fig. 1.** (a) Investigated extra high voltage (HV) DC–DC boost power converter configuration; (b) Equivalent power converter circuit configuration during switch turned ON period; (c) Equivalent power converter circuit configuration during switch turned OFF period.
prototype is implemented with complete controller algorithm written in TMS320F2812 processor. Analyses are carried out on both line and load variations to determine the performance of the whole EHV DC–DC converter system. Numerical simulations with experimental verification results provided in this paper matches closely with the analytical predictions.

2. EHV boost power converter configuration

EHV DC–DC boost power converter circuit diagram shown in Fig. 1(a), represents that the converter consists of N-channel MOSFET as static switch S, diodes (D, D2 ... , D13), voltage-lift circuit with an inclusion of additional capacitors (C, C1, ... , C4) and inductors (L, L0 ... , L3). The voltage-lift gain is obtained by the capacitors (C2, C3 & C4). The capacitor voltage (VC) is built-up by the gain transfer ratio with the four times of the battery input voltage V0 (VC0 = V0). Fig. 1(a) indicates the voltage and current flow directions in the circuit. When the circuit operates in the continuous conduction mode, it is assumed that all components are ideal and capacitors are large enough. The load voltage (V0), load current (I0), supply voltage (V1) and supply current (i0) of the power circuit are depicted in the same Fig. 1(a) and its complete analytical predictions are provided in the next section.

3. Analysis of converter operating modes

Fig. 1(b) explains and provides the details about the instant at which the switch S is turned ON and its corresponding equivalent circuit. At this moment, the instantaneous input current (i1-source current) gets equal to sum of all capacitor and inductor currents except i0 and iC. The load current (i0-load) flows through the circuit depending on the summation of the battery supply voltage V1 and the capacitor voltage Vc. In this circumstance, the capacitors C2, C3 and C4 are charged by the input voltage and increase all inductor currents.

Fig. 1(c) represents about the instant at which the switch S is turned OFF and its corresponding equivalent circuit. The instantaneous input current (i0-source current) equals to zero at this interval. The inductors present in the voltage-lift part which is located on the left-hand side of capacitor C (L1, L2, L3 and L) store the energy, while the capacitor C2, C3 and C4 discharges the stored energy. Therefore, corresponding directions that are leading to charge the capacitor C are shown in the Fig. 1(c). At this situation, the current (I0) flows through the load over the inductor and decreases the current with all the inductors. In steady-state condition, the average inductor voltage will exist over a period as given below:

\[ V_{C0} = V_0 \]

(1)

When switch S is turned ON, the circuit voltages appear as:

\[ V_{C2} = V_{C1} = V_{C4} = V_1 \]

(2)

that also yields:

\[ V_0 = V_{C1} = V_C + V_1 \]

(3)

It should be noted that, the inductor current (i1) is increased during the period when the switch S is turned ON and is decreased during switch S is turned OFF. Therefore, the voltage components V1 as well –V1 OFF, which actually predicts the voltages across the inductor L as:

\[ kTV_1 = (1 - k)TV_{L-OFF} \]

(4)

Whereas, the voltages across inductors (L1, L2 and L3) are determined as:

\[ V_{L1-OFF} = \frac{k}{(1 - k)}V_1 \]

(5)

\[ V_{L2-OFF} = \frac{k}{(1 - k)}V_1 \]

(6)

\[ V_{L3-OFF} = \frac{k}{(1 - k)}V_1 \]

(7)

The capacitor voltage Vc and output voltage V0 are analytically predicted from Fig. 1(c) as:

\[ V_C = V_{C-OFF} = V_{L-OFF} + V_{L1-OFF} + V_{L2-OFF} + V_{L3-OFF} + V_{C2} + V_{C3} + V_{C4} \]

(9)

\[ V_C = 4k[(1 - k)]V_1 + 3V_1 \]

(10)

\[ V_0 = V_C + V_1 \]

(11)

\[ V_0 = 4[(1 - k)]V_1 \]

(12)

Gain transfer ratio of output current and output voltage are predicted as:

\[ i_0 = [(1 - k)/4]i_1 \]

(13)

\[ M_0 = 4/(1 - k) \]

(14)

Finally, the average voltages and currents are described as:

\[ V_C = [(3 + k)/(1 - k)]V_1 \]

(15)

\[ V_{C1} = V_0 \]

(16)

\[ V_{C2} = V_{C3} = V_{C4} = V_1 \]

(17)

\[ i_{0L} = i_0 \]

(18)

\[ i_1 = [k/(1 - k)]i_0 \]

(19)

Table 1

<table>
<thead>
<tr>
<th>Converter type</th>
<th>Output voltage (V0) (Volts)</th>
<th>Output current (I0) (Amps)</th>
</tr>
</thead>
<tbody>
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<td>Classical converter</td>
<td>V0 = [(k/(1 - k))]V1</td>
<td>I0 = [(1 - k)/k]i1</td>
</tr>
<tr>
<td>Proposed converter</td>
<td>V0 = [4k/(1 - k)]V1</td>
<td>I0 = [(1 - k)/4]i1</td>
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Table 2

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<tr>
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<th>Output voltage (V0) Classical converter</th>
<th>Output voltage (V0) Proposed topology</th>
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</tbody>
</table>

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reference voltage $V_{dc}$. Hence the obtained error between the set
obtained from the DC load voltage is then compared with the set
having any additional sensing unit for current. The feedback signal
circuit and notably consists of one voltage sensor feedback without
varies its output voltage from 44.44 V to 400 V.
input voltage is 10 V respectively, while the proposed power circuit
varies its output voltage from 1.11 V to 90 V
in comparison with the classical DC
addition, Table 2 proves the ef
respected to voltage-life transfer gain $k$ for better clari
proposed converter with the classical DC
4. Implementation and analysis of proposed DC–DC boost converter

Table 3, indicates the parameters taken into account for the
numerical simulation test as well as experimental verifications.
Inductance and capacitance values are determined with respect to
the criteria of 5% ($<2$ mV) output ripple requirement as per IEEE
standards [1,19].

Figs. 4 and 5 shows the simulated and experimental results at
the rated condition of the set reference output voltage 120 V with
the load resistance of 44 $\Omega$ and duty ratio $k = 2/3$ (constant) of the proposed EHV DC–DC power converter. It is observed from the
result, as explained above due to the parasitic effects, which veri
Obviously a small deviation is noticeable with the experimental
results that the output voltage is slightly lower than the
set reference and settles at 119.8 V with the negligible loss of
200 mV, which is caused by the self-parasitic effects of power cir-
cept which is practically appreciable. This con

Table 3

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>Input voltage ($V_1$)</td>
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<tr>
<td>Inductance ($L$)</td>
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<tr>
<td>Capacitance ($C$)</td>
<td>5 $\mu$F</td>
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<td>Load resistance ($R$)</td>
<td>44 $\Omega$</td>
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<tr>
<td>Duty ratio ($k$)</td>
<td>2/3</td>
</tr>
<tr>
<td>Switching ($f_{SW}$)</td>
<td>50 kHz</td>
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<tr>
<td>Digital processor</td>
<td>TMS 320F2812</td>
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<tr>
<td>N-channel MOSFET</td>
<td>IRFPC60</td>
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<tr>
<td>$V_{DS}$</td>
<td>600 V</td>
</tr>
<tr>
<td>$R_{DS(ON)}$</td>
<td>0.40 $\Omega$</td>
</tr>
<tr>
<td>$I_0$</td>
<td>16 A</td>
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</table>

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(experimental) by the closed-loop controller when the battery voltage represents a step variation from 10 V to 9 V.

Although the load resistance varies from 48 $\Omega$ to 44 $\Omega$ in the same analytical testing, the output voltage retains the same value of 120 V (set reference) in simulation and settles at 0.005 s, whereas the 119.8 V experimental result settles at 0.850 s as shown in Figs. 8 and 9 respectively. It is observable from experimental test, that the settling time required are little higher than simulated ones due to the parasitic effects. However, the output voltages of both the simulated and experimental results closely match and thereby verify the prediction given in Eq. (12).
Fig. 11. Output current of extra HV DC–DC boost power converter with line-load regulation behavior (Experimental).

Figs. 10 and 11 correspondingly depict both the simulated and experimental output currents under the same line and load perturbation conditions. As expected both the simulated (2.5 A) and experimental (2.495 A) output currents remain the same value irrespective of variation in DC input voltage (battery) from 10 V to 9 V which settles at 0.005 s (simulated) and 0.625 s (experimental) respectively. Furthermore, if the load resistance is varied from 48 Ω to 44 Ω, load current increases from 2.5 A to 2.7272 A which gets settle at 0.005 s in the simulation, where as in the experimental study it increases from 2.495 A to 2.722 A and gets settle at 0.850 s. It is observed that the settling time slightly higher in case of experimental result due to self-parasitic nature gets settle at 0.850 s. It is observed that the settling time slightly higher in case of experimental result due to self-parasitic nature and thereby it is practically appreciable. In addition, in this case both the simulated and experimental results closely match and thereby verify the prediction given in Eq. (13) by satisfying the power-circuit laws.

Further, a complete set of performance outputs obtained from numerical simulation and experimental tests are summarized in Table 4. All operating conditions (duty cycle variation $k = 0.1–0.9$) in the converter performed with efficiency of 100% in simulation and 99% in experimental test with reduced ripple content of 0.22% in simulation and 0.43% in experimental test at the outputs is observed. Finally, the both simulation and experimental test parameters, the output voltage ($V_O$), output current ($i_O$) and efficiency ($\eta$) from the Table 4 are shown in three-dimensional (radar plot) view given by Fig. 12, to confirms the results (simulation/experimental) obtained are very closely matched.

Complete investigation test confirms that the proposed converter produce high efficiency, due to the fact that inclusion of additional passive (L, C) components. This actually reduces the several parasitic effects (L, R, C, and MOSFET switching, conduction etc.) [21]. i.e. losses and increases the voltage transfer ratio gain $k$, which is actually proved in Eq. (12). It is verified by the generated outputs of hardware prototype having losses in the range of milli-amplitude which is practically appreciable. Also, DSP has its own sampling rate to interface with external hardware modules in real time, still the outputs settles less than 1 s in all investigated test.

b) Power Loss Analysis of Proposed DC–DC Converter

In literatures, the parasitic effects due to inductance are neglected in investigations of DC–DC converters. Hence, the RC time constant of converter is always comparable to the switching frequency to attain high efficiency. Therefore, the small parasitic inductance is considered, the results could differ and the inductance connected in the circuit, the current can be expressed by the following equation [21]:

$$i(t) = \frac{V_O}{R}e^{-\frac{t}{RC}} + I_{Load}$$

(21)

where, $V_O$ is the initial voltage difference between the voltage source and the voltage across the capacitor. By considering the parasitic inductor, the input current is given by:

<table>
<thead>
<tr>
<th>Duty ratio ($k$)</th>
<th>Output voltage ($V_O$) volt</th>
<th>Output current ($i_O$) amp</th>
<th>Output power ($P_O$) watt</th>
<th>Input voltage ($V_I$) volt</th>
<th>Input current ($i_I$) amp</th>
<th>Input power ($P_I$) watt</th>
<th>% Efficiency</th>
<th>% Ripple</th>
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Bold values represent parameter taken for experimental and simulation task in closed operation.
Further, \[ i(t) = I_{load}e^{-\frac{i}{2}t \cos \left( \frac{1}{L}C \left( \frac{R}{2L} \right) t \right)} + I_{load} \]
\[ + \frac{V_{0} - \frac{R}{2}}{\sqrt{E} - \left( \frac{R}{2} \right)} 2e^{-\frac{i}{2}t \sin \left( \frac{1}{L}C \left( \frac{R}{2L} \right) t \right)} \]

where, \( I_{load} + I_{o} \) and \( V_{o} \) are the initial current and initial voltage difference between the input voltage and capacitor. The conduction losses of the circuit is directly proportional to the square of the rms value. Based on the above equations, one can easily numerically calculate the ratio of rms current over the average current based on the different parameters, and from which the loss can be calculated. The conduction losses of the MOSFET can be calculated by:

\[ P_{COND} = \frac{I_{ON}R_{DS,ON}}{2} \]  \hspace{1cm} (24)

where, \( I_{ON} \) is the drain current of the MOSFET, when it is ON state, \( R_{DS,ON} \) is the drain-source resistance of the MOSFET, when it is ON state. Therefore, to obtain the average value of the conduction loss, the above Eq. (24) simply multiply by the duty ratio (\( k \)) of the MOSFET.

The switching losses of the MOSFET are due to the non-zero product of the drain current (\( I_{o} \)) and drain to source voltage (\( V_{DS} \)). If the MOSFET were an ideal switch, the rise- and fall time of the current and voltage would be zero and would not have any switching loss. Then, switching losses can be calculated by:

\[ P_{SW} = \frac{T_{SW,ON}V_{OFF}I_{ON}F_{SW}}{2} + \frac{T_{SW,OFF}V_{OFF}I_{ON}F_{SW}}{2} \]  \hspace{1cm} (25)

where, \( V_{OFF} \) is the drain source voltage of the MOSFET, when it is OFF state, \( T_{SW,ON}, T_{SW,OFF} \) are the time to turn the MOSFET ON and OFF state, and \( F_{SW} \) is the switching frequency. From Table 3, N-channel MOSFET ON state resistance \( R_{DS} (0.4) \), C each capacitor (5 \( \mu F \)), \( L \) each inductor (100 \( \mu H \)), and \( f_{s} \) switching frequency (50 kHz) with duty ratio \( k = 2/3 \) (i.e. \( T_{SW,ON} = 2/3*1/50 \) KHz, \( T_{SW,ON} = 1/3*1/50 \) KHz) set for calculate the losses by Eqs. (24) and (25).

Figs. 13 and 14 depicts the variation of normalized conduction and switching loss when parasitic \( L \) changes (simulation/experimental). It is observed, that the conduction losses are dramatically reduced with variation of inductance profile (at 100 \( \mu H \)). Relatively, the switching loss is reduced and minimal at the resonant point (at 100 \( \mu H \)) and further increased with variation of inductance profile. It is concluded that, the increasing parasitic effects of power converters can be overcome by inclusion of additional passive components (\( L \) and \( C \) i.e. voltage lift technique) within the power circuit without any additional external compensation network/circuitry [1–9,21].

Finally, the obtained performances higher output voltage and higher efficiency, reduced % ripple and faster settling time (Table 4), which verifies that the proposed DC–DC converter (hardware...
prototype) has better power density factor as per standard [22–24]. Proving exact viability for parasitic compensation and suits the high voltage industrial needs.

5. Conclusion

Experimental implementation of hardware prototype EHV DC–DC boost power converter based on DSP TMS320F2812 process controller is described along with the relevant theoretical validations in this manuscript. The DC–DC power converter circuit integrated with the voltage-lift technology generates a high performance output-voltage compared to the conventional DC–DC boost converter whereas the duty ratio remains the same. This approach significantly overcomes the parasitic effects and reduces ripples at the output waveforms (voltage/current). A close loop controller with only one voltage sensor feedback, algorithm is developed to maintain the output voltage requirements under the line and load perturbation conditions. Simulation results provided in this manuscript are in accordance with the experimental results that are verified by the theoretical predictions. Hence the analyzed EHV DC–DC converter is suitable for the industrial applications, where the high-voltage becomes mandatory with reduced ripple at the output.

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