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A SIMULATION MODEL TO CHARACTERIZE PHOTOLITHOGRAPHY PROCESS OF A SEMICONDUCTOR WAFER FABRICATION

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ABSTRACT

The pressures on semiconductor manufacturers due to cost considerations, rapid growth of process technology, quality constraints, feature size reduction, and increasingly complex products are requiring ever higher efficiency from manufacturing facilities. The complexity of manufacturing high capacity semiconductor devices means that it is impossible to analyze the process control parameters and the production configurations using traditional analytical models. There is, therefore, an increasing need for effective models of each manufacturing process, characterizing and analyzing the process in detail, allowing the effect of changes in the production environment on the process to be predicted. The photolithography process is one of the most complex processes in semiconductor manufacturing. Using state-of-the-art computer simulation and a structured modelling methodology a generic model of photolithography flexible manufacturing cells has been developed and used to mimic the actual performance of the tools. Comparison of the output from the model with data from the plant shows the quality of the model. This paper discusses the technique used to develop the simulation model and includes a details on the structured modelling approach employed to develop reusable generic model for optimizing photolithography process parameters.

KEYWORDS: Photolithography Process, Simulation, Semiconductor Manufacturing.

1. INTRODUCTION

In *A Tale of Two Cities*, Dickens begins, "It was the best of times, it was the worst of times…." [1]. Never has more reliable semiconductor power been available to the consumer at such a low price, and never have the pressures on the manufacturers of these devices been more severe. [2] In essence, it is the best and worst of times. The market demands impose further complexity into each of the manufacturing processes in an effort to meet the demands. Semiconductor manufacturing is one of the most complicated manufacturing systems in terms of technology and procedure. Traditional industrial engineering analysis techniques through mathematical models or even deterministic models to study manufacturing areas are simply not adequate to analyze these complex manufacturing environments. These have to be modelled and optimized by means of powerful techniques such as simulation and system analysis approaches (e.g. IDEF0, design of experiment), in order to properly model the dynamics as well as variability of the system. The photolithography process is considered the most complex process in the wafer fabrication due to complex technology, critical dimensions, and re-entrant flow [3]. Thus it is often the semiconductor manufacturing bottleneck and it has a significant impact on overall factory performance.

Much research has been carried out into various aspects of the electronic manufacturing in general [4] and semiconductor in particular [5]. Some research has investigated in detail specific process parameters such as cycle times [6][7]. From the literature as well as industrial sources, there is no overall methodology exists through which a systems approach can be employed. Few researches have been published on photolithography process in semiconductor manufacturing [8]. This paper presents a generic systematic methodology for optimizing photolithography process parameters. The proposed methodology integrates three techniques to generate efficient model for analysis, control, and optimization of photolithography tools.

2. PHOTOLITHOGRAPHY PROCESS

The wafer fabrication processes by which wafer are manufactured can be divided into six basic steps: cleaning/oxidation, photolithography, etching, implantation, diffusion, and metrology (Figure 1). The number of operations in wafer fabrication can be well into the hundreds for a complex component such as microprocessor. Added to that, the operations may vary widely depending on product configurations or the technology in use. Product moves through the factory in lots, often of a constant size based on standard containers used to transport wafers. Photolithography involves the processing of wafers in order to build up the layers and patterns of metal and wafer material to produce the required circuitry.

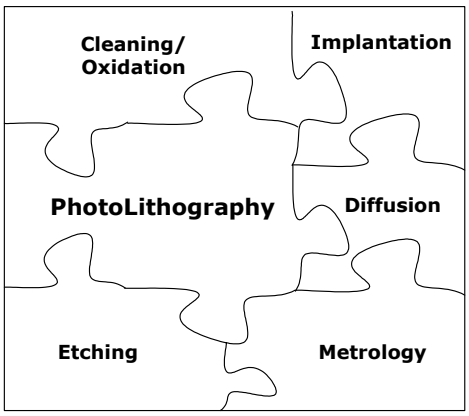

Figure 1. Wafer fabrication jigsaw

During the photolithography process the circuit pattern is to be transferred from a mask onto photosensitive polymer and finally replicates the pattern in the underlying layer. The object of this process is the accurate and precise definition of a three-dimensional pattern on a semiconductor substrate.

The basic photolithographic sequence is shown in figure 2. Typically, the wafer lot to be processed goes through a coating operation, where the wafers are coated with photo-resist substance. The wafer lot is then moved to the expose operation where the patterns are photographed on the wafers. The exposed wafers move over to the developing operations. Once these steps are completed, the lot typically is moved to post-photolithography analytical operations. The amount of metrology is dependent on the product and the layer being processed. Details of the three basic steps in photolithography are described in the modelling section.

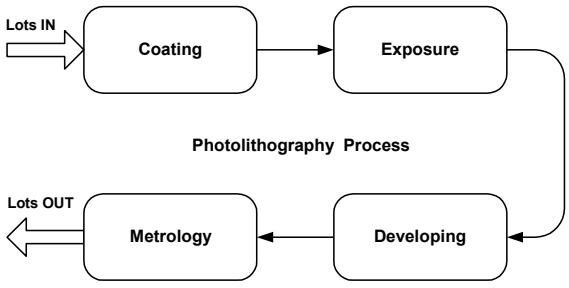

Figure 2. Simplified diagram of typical photolithography process flow

3. PHOTOLITHOGRAPHY MODEL

The aim of the photolithography process tool model is to offer the manufacturer a systematic methodology to understand better the behaviour of the process and achieve optimal operating conditions. The model presents a comprehensive integration between three analytical techniques such as integrated computer aided manufacturing definition ICAM or IDEF, simulation, and design of experiments analysis in order to accomplish the following objectives:

1. To build an effective hybrid model to characterise photolithography process;
2. To determine the significance of the impact of process control parameters;
3. To enhance the process performance by determining the optimal combinations of process parameters;
4. To provide a state-of-the-art simulation model to economically examine the process performance under different production scenarios.

The coming sections will include briefly the process description and the modelling approach used in the methodology, see figure 3.

3.1 Photolithography Process Constraints

The main constraints imposed on the model due to the complex procedure in the photolithography operations come into two main groups; constraints due to the technology complexity, and constraints due to production. The first group includes operations sequence, setup times, processing times, and metrology. While the other group involves the lot integrity, re-entrant flow, product/layer sequence, storage area (buffers), maintenance breakdowns (preventive and unscheduled). The main buffers are located in front of every manufacturing cell and the exposure operation within each cell.

3.2 Selected Process Parameters

In most of the cases, the photolithography process can run uninterrupted after a lot of wafers is loaded on the manufacturing cell. In this study, the authors have studied the effect of some key process control parameters (e.g. wafers start (WS), number of

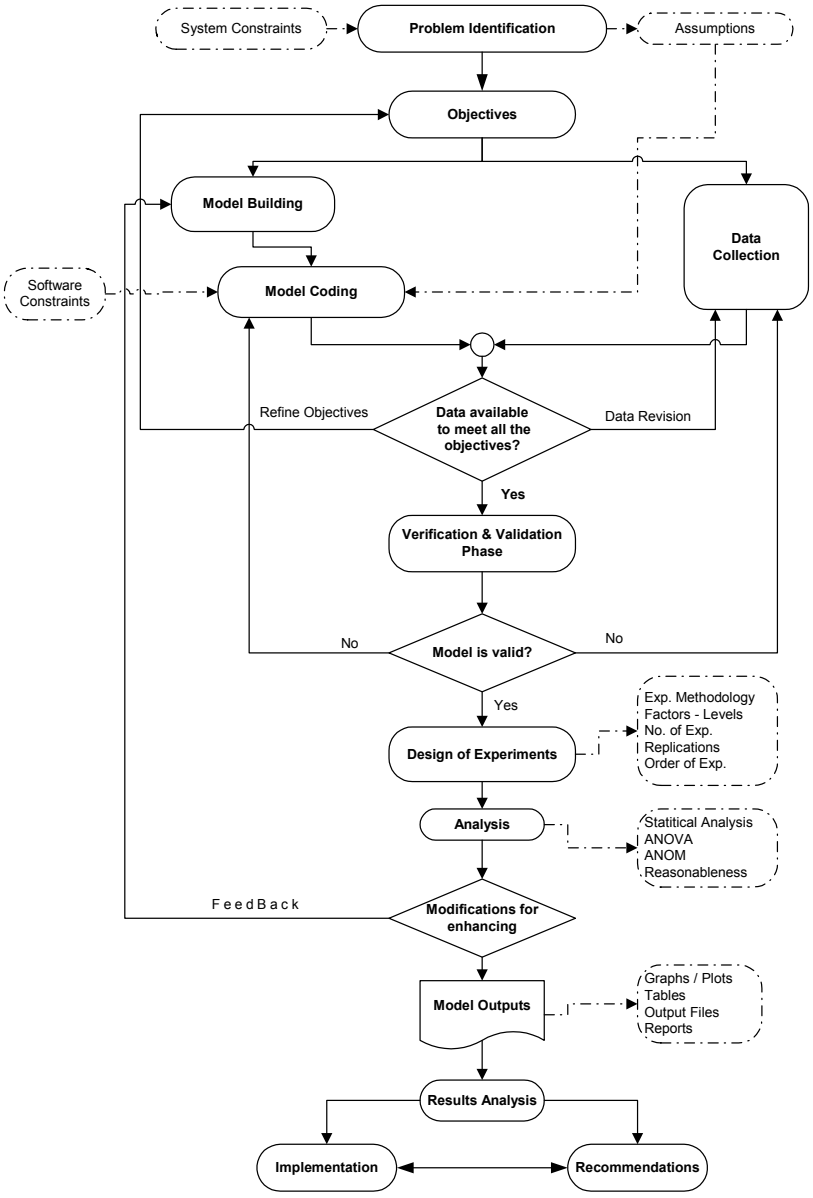

Figure 3. Methodology Steps

products/product-mix (PM), dispatching rules (product sequence), and stepper buffer size (BS)) on the performance of photolithography flexible manufacturing cell. The performance measures of interest are makespan, cycle time, and utilization.

3.3 IDEF0 Model of Photolithography Process

The semiconductor processes are characterized by: the complexity of operations, large amount of data, cyclic nature of operations, and rapid changes in product configurations. One of the most effective tools to model those complex industrial systems with diversity and interdisciplinary nature is IDEF [4]. IDEF0 part of IDEF has been selected for modelling because it offers a structure of a top-down approach which is simple to use and provide a good means of describing the functional processes within complex manufacturing environment. Process modelling in IDEF0 starts with a basic function and then breaks it down into sub-levels. The basic element of an IDEF0 model is called a function block, which can be decomposed into more detailed sub-function blocks further down the hierarchy, while the lower-level function blocks describe the supporting subsystems. Further information about IDEF0 can be found in references [9][10].

Photolithography lays down patterns on layers, allowing other processes (e.g. oxidation, etching, ion implantation) to produce the required circuit devices and interconnections. In this way it is the central process within the manufacturing plant and each will pass through many times before completion. Figure 4 shows the top level of the developed IDEF0 model for wafer fabrication and indicates the sequence of processes, the inputs such as Process Planning (PP) data (raw materials, schedules), the control such as process characteristics and process factors, the mechanisms (machine, operator, software) and the outputs (finished products).

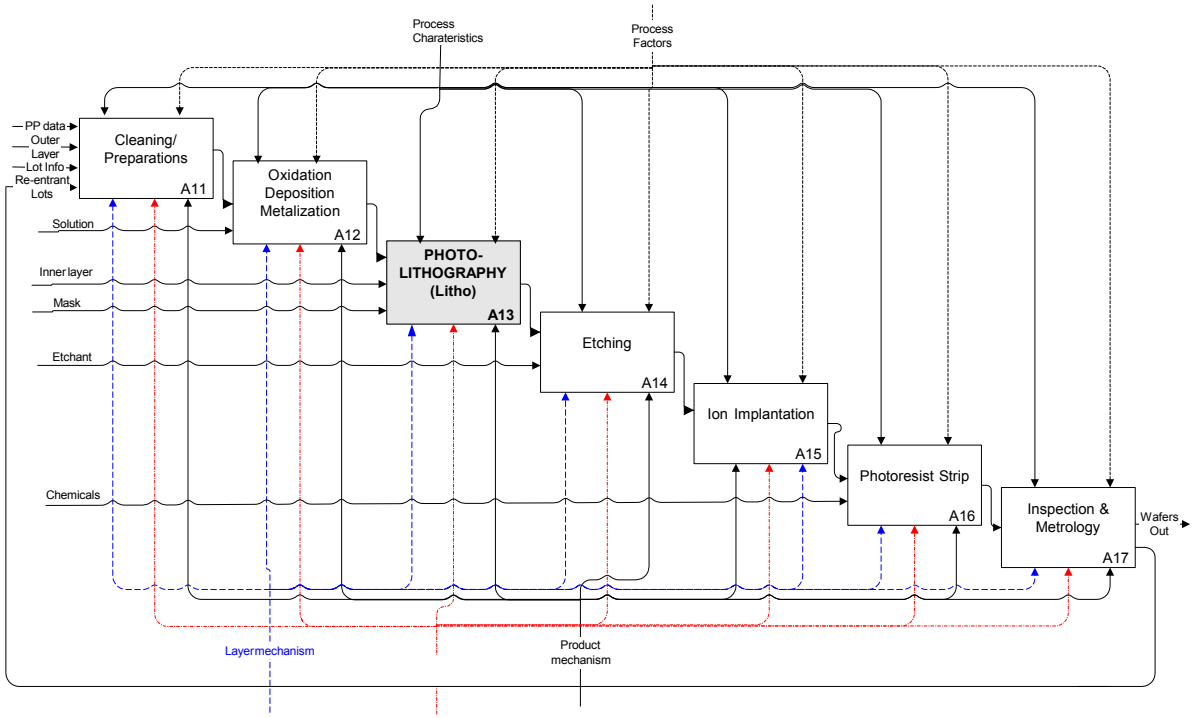

Figure 4. Top level of systematic developed model for wafer fabrication

The focus in this research on photolithography process (A13) comes in the second level of details (B-level) for photolithography tools and operations. The generic model of photolithography tools in figure 5 has been used to detail the operations in the photolithography process.

Most photolithography processes have a similar process flow within limited variations. The process has mainly three sets of operations includes "Spin/Coat" operations, "Align/Expose" operations, and "Develop" operations as illustrated in figure 6. Every set of operations of the photolithography tool have modelled in detail as follows to be used within the model.

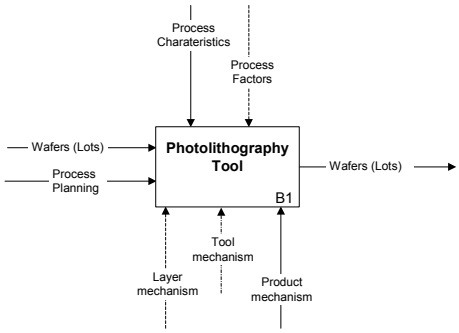

Figure 5. Level B, photolithography tool block (B1)

3.3.1 'Coat/Spin' Operations (B12)

In the "Coat/Spin" set of operations (figure 7), all moisture is removed from the wafer surface at high temperature.

The wafer is then cooled before the photo-resist is dispensed at the centre of the wafer and spun over the entire surface. Edge Bead Removal (EBR) is carried out before the photo-resist is healed. Next operation aims to remove solvent out of resist and then cools wafer again for transfer to the exposure process.

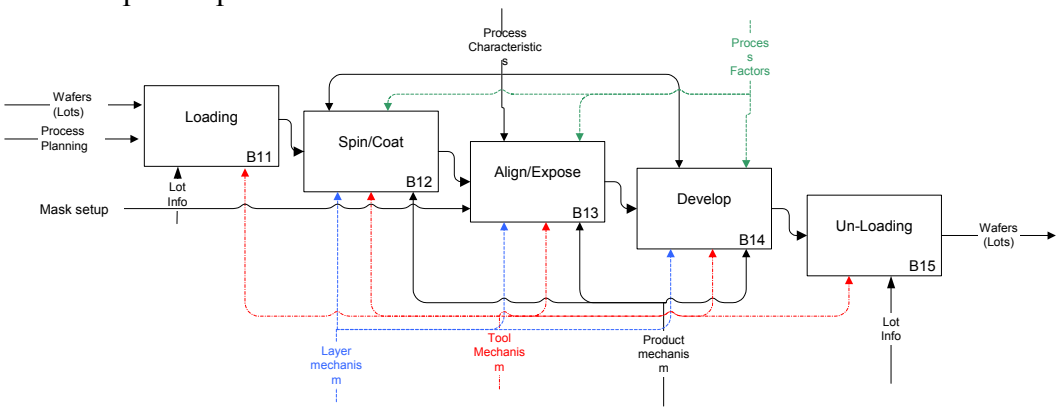

Figure 6. Photolithography process steps second level

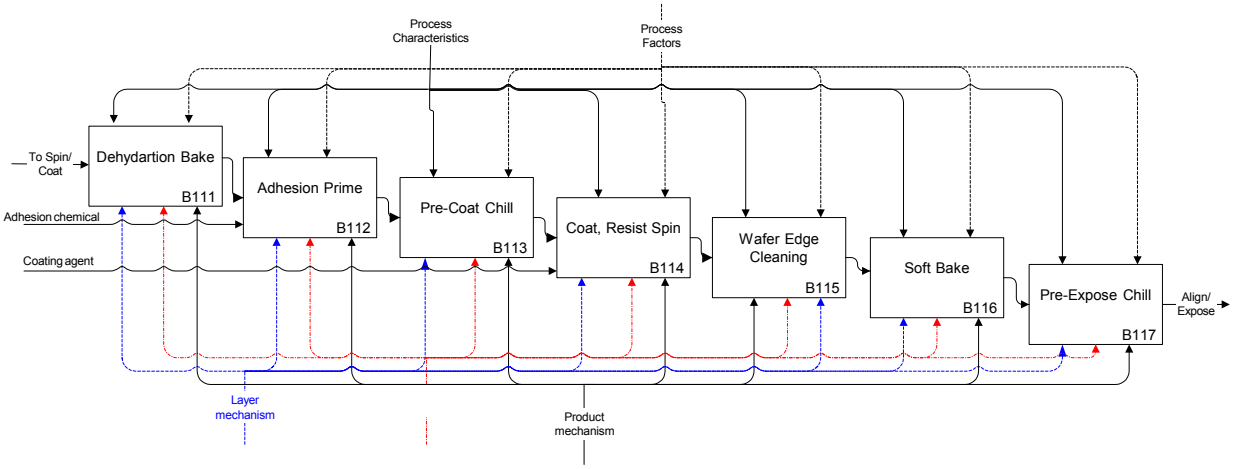

Figure 7. IDEF0 of Coating Operation (B12 Block)

3.3.2 'Align/Expose' Operations (B13)

As dimensional accuracy is critical there are several alignment operations (figure 8). Each mask must be defined carefully upon insertion to the system, and then each wafer must be held in the correct position and indexed across the exposure location to allow the pattern for each layer on the wafer to be transferred accurately over previous exposures. It is worth to mention that there is a buffer (storage area) in front of the exposure operation. Buffer capacity varies based on the manufacturing cell design and planning configurations.

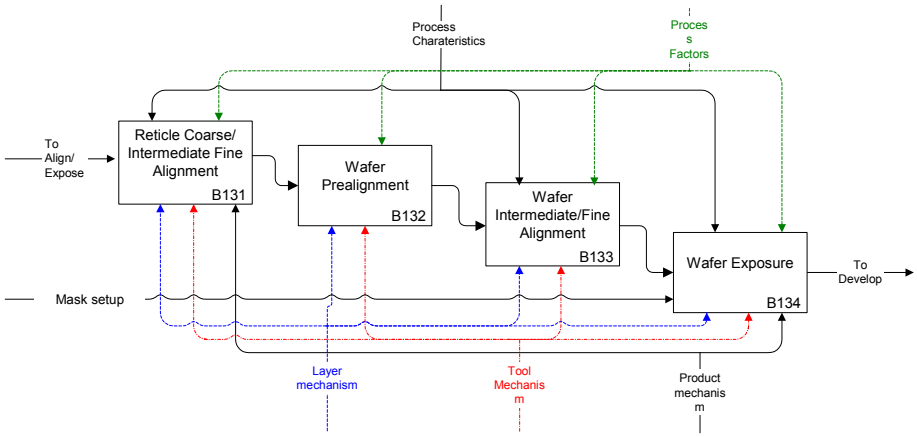

Figure 8. IDEF0 of Exposure Operation (B13 Block)

3.3.3 'Develop' Operations (B14)

In developing, (figure 9) the edge of the wafer is first cleared using a small scale exposure tool. Post-exposure bake is required to fix the exposure before chemicals are applied to remove unwanted film from the wafer. The wafers are finally rinsed, spun to dry, and then cooled down for transport.

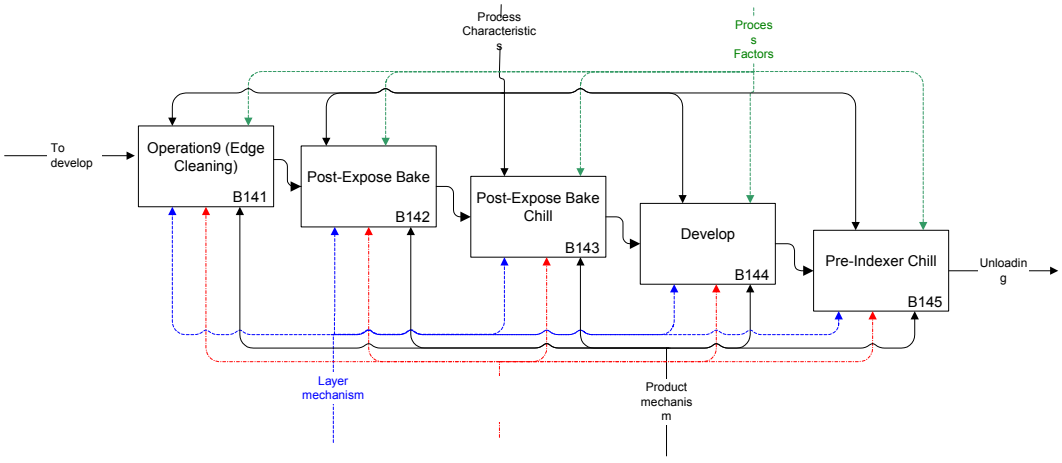

Figure 9. IDEF0 of Developing Operation (B14 Block)

The IDEF0 model was verified using industrial expertise in the industrial partner to ensure that the conceptual model is realistic before model coding step.

4. SIMULATION MODEL

Once the conceptual modelling phase was complete the simulation model building started by the assumptions and reviewed the constraints with the manufacturing team [11]. The real-time simulation model aims to provide a reusable generic model of the photolithography process tools.

4.1 Simulation Assumptions

Assumptions made were not to allow pre-emption, use default lot size of 25 wafers, ignore the initial setup time, operator is always available to intervene if necessary, and consider the unscheduled maintenance delays have exponential distributions. It is worthy to mention that the data collection process has been going on while model building and model coding phase with the help of the manufacturing and planning staffs. The information gathering and analysis included data such as equipment dedication (i.e. certain tools are selected to perform specified tasks), number of steps in every operation, etc. Prior manufacturing experience and input obtained from the production planning and development groups also played a major role in setting up the framework of the model.

4.2 Simulation Output

A host of simulation output measures can be obtained from the model which may be useful in the characterisation of the photolithography cells. Of these the following were considered the most relevant:

a) Process equipment throughput time
b) Photolithography step throughput time
c) Work In Process (WIP) inventory level in every step
d) Cycle Time per wafer/lot (CT)
e) Equipment utilization

4.3 Model Verification and Validation

The strength of decisions made based on the simulation model is direct function of the validity of this data [12], hence the need for efficient and objective methods to verify and validate the model is increasing. The verification and validation of the model took place as a continuing process [11]. The simulation model has been verified using three approaches.

The first approach compares the output of the simulation model with actual data from the manufacturing floor. The outputs also compares to the existing models, although these models cannot provide same capabilities for high wafer starts. The simulation model output shows a comprehensive trend on throughput time criterion as shown in figure 10. The gap between simulation output to actual data about 4%.

The second approach tends to check the output through a trace file, which consists of detailed output representing the step-by-step progress of the simulation model over the simulated time. In addition a decomposition approach (i.e. to verify every group of blocks) has been applied to verify the model. This approach was efficient to detect the errors in the model and make sure that every block functions as it should. Moreover, this allows detection of subtle errors.

Finally, the third approach is based on reasonableness of the model outputs. This approach considers experts and manufacturing people, as they are the reference to validate the model results on reasonableness.

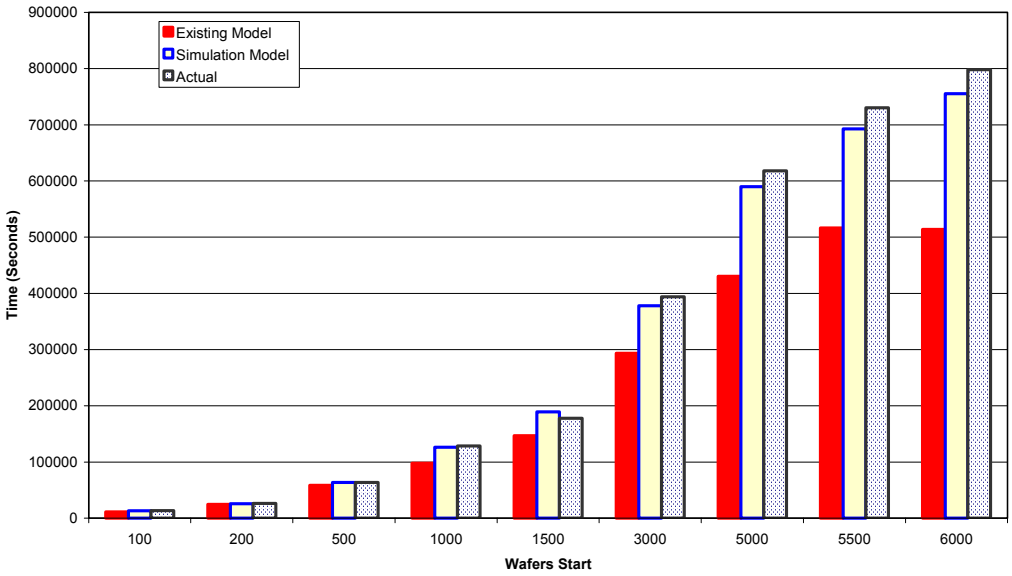

Figure 10. Comparison between simulation output, actual data, and deterministic models

5. SIMULATION EXPERIMENTS

Experimental design framework was adopted to provide a convenient procedure for conducting the main simulation runs. Furthermore, it helps in finding suitable factor (level) combinations to optimize performance measure estimates. In order to study the impact of the selected control parameters, standard orthogonal array experiments (L_{25}) has been conducted to determine the factor combinations that will optimize the defined objective. In addition, statistical analysis has established the relative significance of individual factors in terms of their effect on the objective function. Each parameter has five different levels recommended by the production planning staff.

The results obtained from the matrix experiment were analyzed using statistical analysis techniques. The main formulas used for calculating the main effect of factors are given in Phadke [13]. Based on the analysis of means (ANOM), the near optimum level for each factor can easily be identified as the level that results the minimum average throughput time (TPT) in the factor-level range, figure 11. Accordingly, the predicted factor level combination that should optimize the average makespan is WS4, PM1, PS4, BS2, which is interpreted to mean the wafer starts should be 3750, and product-mix is one product, the dispatching rule is the wafer with less layer number comes first, and stepper buffer size equal to three.

The analysis of means reveals the relative magnitude of effects of changes in each factor on the throughput time per wafer. The product-mix is seen to affect the TPT the most, followed by wafers start. However, a better feel for the relative effects is obtained by conducting the analysis of variance (ANOVA). The ANOVA (table 1) shows the significance of individual factor by establishing the relative magnitude of the effect of each factor on the objective function. From the ANOVA tableau, the relative effects of the factors WS, and PM are seen to be highly significant. This is agreement with the ANOM results.

A number of simulation sensitivity analyses were performed. These included experiments to analyze the variation in cycle times through each of the litho steps in order to detect the process bottleneck(s). The results are shown in figure 12.

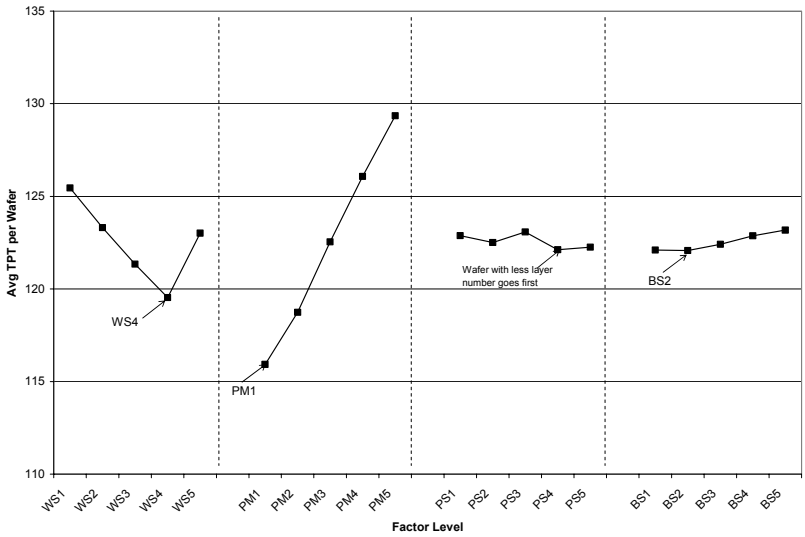

Figure 11. Analysis of means of factor main effects (ANOM)

Table 1: ANOVA matrix

Factor	Degree of Freedom (DOF)	Sum of squares (SSB)	Mean square (SSB/DOF)	F
WS	*4*	*0.499298*	*0.124825*	*16.126*
PM	***4***	**2.946854**	**0.736714**	***95.1765***
PS	4	0.023777*	0.005944	
BS	4	0.023888*	0.005972	
Error	8	0.076183*	0.009523	
Total	24	3.57		
(Error)	(16)	(0.123848)	(0.0077405)	

* Indicates the sum of squares added together to estimate the pooled error sum of squares, indicated by parentheses. The F ratio is calculated using the pooled error mean square.

6. RESULTS DISCUSSION

Experimental design paradigm has been used to gain better understanding of the behaviour of the selected process control parameters. Based on the ANOM plot in figure 11 and ANOVA detailed in table 1, the process control parameters (i.e., the number of wafers start and product-mix) have a statistically significant impact on the total throughput time and in particular the TPT per wafer. In contrast, the parameters such as product sequence and stepper buffer size are not seen to be statistically significant. The results suggest that experimentation should focus attention on the alternatives available for the product-mix and wafers start and only then the other parameters for improving the shop global performance. The use of the experimental design procedure provides an expedient platform for quickly focusing on the parameters that need to be given priority. However in practice, the product-mix cannot be set to one as recommended but it provides the planning staff with an indication of significant effect of increasing the product-mix factor.

The sensitivity study of the variation in cycle times through each step in the photolithography process helps to identify the bottleneck steps in the manufacturing cell. The experiments can be carried out for many combinations of wafer starts, layer-mix, product-mix, and different dispatching rules in order to optimize the throughput time. Further sensitivity analysis has been conducted on studying the impact of increasing wafer starts per product on the process performance.

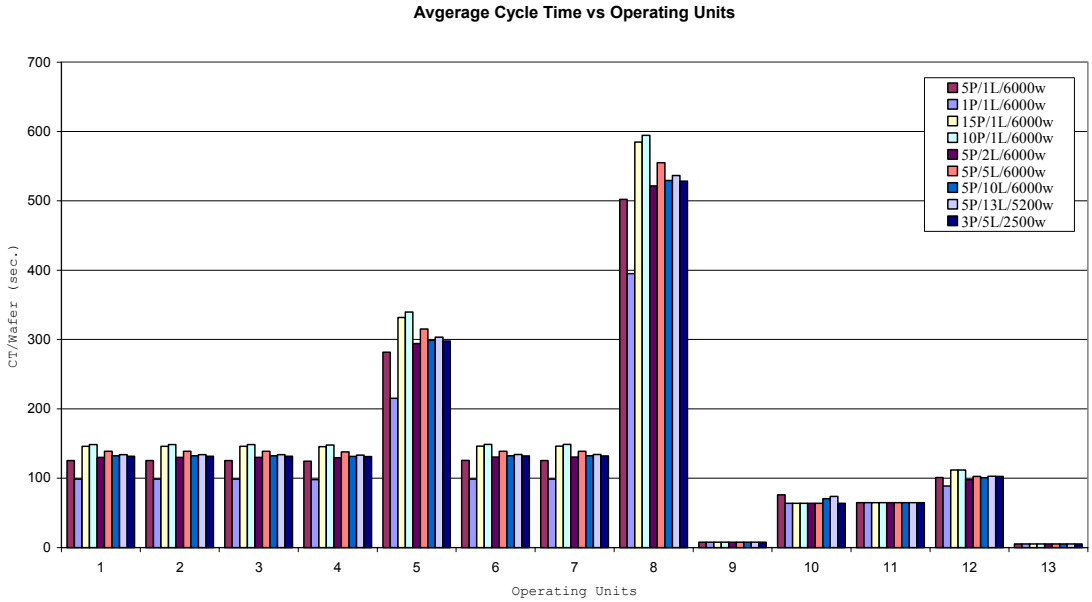

Figure 12. Variations in photolithography steps average cycle times

Generally speaking, the quality of any simulation approach is measured in at least two dimensions: (1) how close the output comes to the real system if it can be measured; and (2) how much computer time is required to solve problems of a given size [3].The simulation model has shown excellent results and given better understanding of the cell behaviour under various operating conditions. The quality of the output has been verified with actual floor data of similar conditions. The computer time required to run the simulation model for one experiment was economic, less than three minutes on Pentium IV processor.

7. CONCLUSIONS

The photolithography process is one of the most complex processes used in wafer fabrication. Process optimization is a critical task in such complex processes. The paper presents an approach including three effective techniques namely; IDEF0, simulation, and experimental design procedure. This systematic approach has been successfully developed to characterize the photolithography process as well as optimize selected process control parameters. An IDEF0 modelling technique has been used to understand the process steps and model the system in standard format. IDEF0 technique proved to be useful and flexible system description tool offering structure modelling approach to wafer fabrication. It enabled the approach to be applied in stages by analysing the photolithography process individually and as a whole.

The effective use of experimental design procedure in optimizing the process control parameters has a significant impact on decision-making within complex flexible manufacturing environments. The role of decreasing product-mix (whenever it is possible) should be taken for granted as a direction for performance improvement. The proposed design of experimental could optimize the level for different process control parameters which help manufacturing staff to focus on setting priorities among the process parameters.

The development of a reusable generic simulation model to characterize the photolithography process in wafer fabrication has provided a robust tool to examine the impact of various

production changes on the photolithography process. The model has been successfully verified and validated and the results presented used to assist photolithography area in a new wafer fabrication. The model has also reduced the turnaround time in evaluating the impact of policy decisions on the manufacturing performance.

REFERENCES

[1] C. Dickens, *A Tale of Two Cities*, Book the First, Chapter 1, line 1, edition (1994).

[2] C. Hilton, *Manufacturing Operations System Design and Analysis*, Intel Technology Journal, 4th Quarter '98, 1998.

[3] A. Arisha, *Intelligent shop scheduling for semiconductor manufacturing*, PhD thesis submitted 2003, Dublin City University, Ireland, (2003).

[4] A. Doniavi, *Computer aided systems engineering approach to electronic manufacturing*, PhD thesis, University of Bath, UK, (1999).

[5] R. Uzsoy, Chung-Yee Lee, and L. Martin-Vega, *A review of production planning and scheduling models in the semiconductor manufacturing, Part I,* IIE transaction on scheduling and logistics, Vol. 26, pp 44 – 55, (1994).

[6] Akcali, E., Nemoto, K., and Uzsoy, R., *Quantifying the Benefits of Cycle-Time Reduction in Semiconductor Wafer Fabrication*, IEEE Transactions on Electronics Packaging Manufacturing, Vol. 23, pp 39 – 47, (2000).

[7] Y. Lee, S. Kim, S. Yea, and B. Kim, *Production Planning in Semiconductor Wafer Fab Considering Variable Cycle Times*, Computer Industrial Engineering, Vol. 33, No. 3 – 4, pp 713 – 716, (1997).

[8] D. Williams, and D. Favero, *Dynamic Deployment Modelling Tool for Photolithography WIP Management*, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp 55 – 58, (2002).

[9] United States Air Force, *Integrated Computer Aided Manufacturing (ICAM)*, Architecture Pt II, Vol. IV, Function Modelling Manual (IDEF0). Air Force Materials Laboratory, Wright-Paterson AFB, Ohio, 45433, AFWAL-TR-81-4023, June (1981).

[10] L. A. Haines, *An IDEF0 representation of the instructional system development (ISD) process*, IEEE Proceedings of the National Aerospace and Electronics Conference, V2, pp. 806 – 811, (1990).

[11] J. Banks, *Introduction to Simulation*, Proceedings of the Winter Simulation Conference J. A. Joines, R. R. Barton, K. Kang, and P. A. Fishwick, eds., (2000).

[12] N. Nayani, and M. Mollaghasemi, *Validation and verification of the simulation model of a photolithography process in semiconductor manufacturing*, Proceedings of the 1998 Winter Simulation Conference, pp 1017- 1022, (1998).

[13] M. S. Phadke, *Quality Engineering Using Robust Design*, Prentice-Hall International, Englewood Cliffs, NJ, (1989).