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An Investigation into Appliance Durability in the Presence of Power System Disturbances

Steven R. McGovern, B.Sc. (Eng), HDipEE

Submitted for the Qualification of Master of Philosophy



Dublin Institute of Technology

Supervisors: Mr. Michael Farrell

Dr. Eugene Coyle

School of Control Systems and Electrical Engineering

April 2004

Declaration

I certify that this thesis which I now submit for examination for the award of MPhil, is entirely my own work and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

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Steven McGovern

Date 30th April 2004

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Abstract

The increased trend towards miniaturisation and greater efficiency in electronic equipment has also resulted in increased susceptibility to power system disturbances. Such equipment has become less tolerant to supply transients and variations and as a result there has been an increase in consumer product damage complaints. Greater consumer awareness has seen power quality become a major issue for both the domestic user and the utility companies. Arising from these issues an approach from the Electricity Supply Board of Ireland was made to engage into an investigation of the effects of power quality disturbances at the low-voltage domestic level.

On commencement of the research a study was made of power quality disturbances and the associated electromagnetic compatibility immunity (EMC) standards. Test limits and regimes from these standards have been used to carry out an investigation into the disturbance withstand capabilities of television, VCR and personal computer power supplies. Owing to the prevalence and widespread use of switch-mode power supplies in powering electronic apparatus, a study was made into the typical topologies and operation of the switch-mode power supply and a computer model was created using PSpice circuit simulation software. By simulation the model was used to assess how the power supplies perform when such disturbances were injected at their input.

A typical medium-voltage 20 kV section of the utility's distribution network was also modelled in Matlab. The network was subjected to lightning surges and switching operations at various points on the network. The surge levels experienced were observed and the results were analysed to determine whether consumers at the low-voltage level would experience damage to their equipment.

Seminally, the results obtained are interesting in light of the current discussion on the introduction of the EN 50160 standard which proposes a significant increase in withstand limits which will have a major impact on equipment manufacturers, utility companies and ultimately, equipment end-users.

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Chapter 1 Introduction

1.1 Thesis Overview

The work of this thesis arose from a proposal by the Electricity Supply Board (ESB) of Ireland for investigative work to be carried out into the failure of domestic appliances in the presence of supply transients. The ESB indicated that there may be an issue in regard to the robustness of domestic appliances to withstanding transient disturbance phenomena that may occur in the supply networks. In particular it was indicated that some customers had reported damage to common domestic appliances such as televisions, video-cassette recorders, audio equipment, microwaves and personal computers and linked this failure to a supply disturbance e.g. lightning, switching or voltage dips on the network.

This type of problem is not new and has been actively researched over the years, [1], [2], in line with growth in the use of electronic equipment. The proliferation of electronic equipment has made consumers more aware of power system disturbances that typically went unnoticed in the past.

A common factor amongst these appliances is the large number of electronic components they contain and the fact that their interface to the mains is generally a switch-mode power supply (SMPS). As this interface is the first part to see the disturbance, it is the most vulnerable part of the appliance and it was decided that the work would concentrate on investigating the performance of switch-mode power supplies in the presence of supply transient disturbances.

A broad approach is taken in investigating the problem, the research commencing with a study into power quality i.e. types of disturbances, causes, protection and resulting costs. A review of power quality and its surrounding issues are discussed in Chapter 2.

As robustness was an issue the next step was to identify the appropriate standards to which the supplies are manufactured and from these the recommended withstand levels of the supplies to various power quality tests were to be ascertained. The appropriate disturbance standards and their test regimes are discussed in Chapter 2. Because of the nature of the project indepth knowledge of the relevant standards and associated test

regimes was required. The accompanying workbook to this thesis provides further details and descriptions of the standardisation process and structuring as well as the relevant standardisation bodies.

Having identified switch-mode power supplies as being the most vulnerable part of the appliance it was essential that a thorough investigation be conducted into the design and operation of these power supplies. The switch-mode power supply and its variants are discussed in detail in Chapter 4.

Having become familiar with the operation of the SMPS and the standards to which they are constructed, the next stage in the research was to subject different SMPSs to a series of tests to assess their withstand capabilities. A number of typical supplies, from televisions, VCRs and personal computers, were obtained and using a Schaffner Best EMC disturbance generator were subjected to the transient tests described in the standards. Harmonic emission analysis to assess the effects the power supplies have on the supply system was also carried out for these power supplies. Chapter 5 outlines the tests conducted and discusses the results obtained.

In order to gain a greater appreciation of the physical results obtained a computer model of a typical switch-mode power supply was developed and subjected to simulations of the electromagnetic compatibility (EMC) disturbance tests. As a greater number of test measurement points could be accessed this facilitated a better insight into the behaviour of the supply in the presence of supply disturbances. This simulation work and the results obtained is discussed in Chapter 6.

Finally the last stage in the research was to try to establish, through simulation of a typical medium-voltage (MV) network, that level of transient surges a low-voltage (LV) customer is likely to see. A section model of a typical MV/LV network was subjected to switching and lightning effects and measurements were made at the LV terminals to observe the level or surges that would be seen by the customer. The results were analysed and compared with the withstand levels from the physical EMC tests. The modelling of the MV distributor is discussed in Chapter 7.

A review of previous research carried out relating to the thesis topic was also made. As well as using the internet, published journals from the Institute of Electrical and Electronics Engineers (IEEE) [3] and the Institution of Electrical Engineers (IEE) [4] in

the UK provided the best source for information on previous work in the area. The more significant sources were from studies carried out in the USA.

Chapter 2 Power Quality and Standards

2.1 Introduction

Power Quality is generally referred to as any electrical disturbance that can adversely affect the performance of a customer's load or power equipment. These disturbances are classified according to the changes which they cause to the normal power voltage and/or current waveshapes using power quality terms e.g. sags, swells, transients etc. The standards to which equipment is manufactured specify the withstand limits of equipment to these well-defined disturbances. As the focus of this research is the investigation into the mechanism of failure for equipment (in particular domestic appliances) in the presence of supply disturbances, a thorough knowledge of the types of disturbances and the associated equipment standards is required.

This chapter discusses power disturbances in the context of power quality. A brief discussion on the most common disturbances experienced at the low voltage consumer level is presented as well as information on the associated immunity standards that domestic equipments are required to be tested and manufactured to withstand. The accompanying workbook provides further background information on the structure of standards and the standardisation process.

In addition the effect of the appliances on the supply in terms of harmonic emissions content is also discussed. The relevant harmonic standards and the harmonic emission limits for the equipment being considered are identified.

2.2 Sags/Swells and Interruptions

A sag is basically a reduction in the a.c. voltage over a number of supply cycles, whereas a swell is an increase in the voltage. An interruption is a total loss of the supply voltage for a period of time. Table 2-1 outlines the definitions, causes, effects and additional details relating to these disturbances.

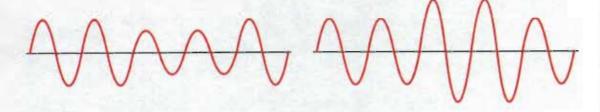


Figure 2-1 - Voltage Sag and Voltage Swell waveforms

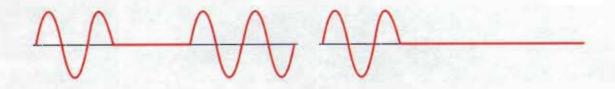


Figure 2-2 - Interruptions in the Supply Momentary (left), Temporary/Sustained (right)

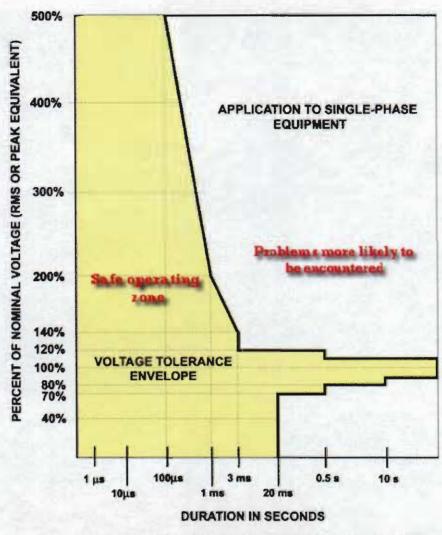
Definitions:	Sag: (also referred to a 'voltage dip') is a momentary RMS reduction in		
	the normal a.c. voltage level with duration ranging from a half-cycle to a		
	few seconds [5]		
	Swell: is a momentary RMS increase in the normal a.c. voltage level with		
	duration ranging from a half-cycle to a few seconds		
	Undervoltages/Overvoltages: same as sags and swells but have longer		
	durations and therefore are usually more harmful to equipment		
	Interruption: the complete loss of voltage for a period of time, be it		
	momentary (between a quarter cycle to a few seconds), temporary		
	(several seconds to a few minutes) or sustained (indefinite time period)		
	[6]		
Sources:	Utility supply or customer loads. Power failures, storms, major equipment start-up/shutdown (such as motors), short-circuits on the		

	system or under-sized electrical circuits. [7] Lightning strikes, accidental digging of power lines or animals/trees on power lines
Effects:	Memory loss, data corruption, damaged power supplies in electronic equipment. Flickering may also be observed Interruptions: depending on the duration, shutdown and data corruption are most likely
Protection:	Uninterruptible Power Supplies (UPSs), back-up generators
Standards:	U.S.: IEEE 1159 Europe: EN 61000-4-11

Table 2-1 - Sags/Swells and Interruption information

2.2.1.1 The CBEMA Curve

The Computer and Business Equipment Manufacturers Association (CBEMA) have developed a voltage tolerance curve to categorise the severity of a voltage disturbance. Revised by the Information Technology Industry Council (ITIC) in 1996 it will continue to be referred to as the "CBEMA Curve." As seen in Figure 2-3 the curves, define an upper and a lower bound on the types of disturbances electrical equipment is likely to tolerate. It plots disturbance magnitude against duration and indicates at what point a voltage disturbance (commonly a sag or swell) is likely to disrupt or damage equipment. Voltage levels and durations at the equipment terminals, within the tolerance envelope represent acceptable energy being delivered.



NEW ITIC (CBEMA) CURVE (1996)

Figure 2-3 - CBEMA Curve

As can be seen from the curve, disturbances (usually sags, swells and surges) lasting for time periods greater than one cycle and of significant voltage variation will result in failure and possible damage to the equipment.

The CBEMA curve is applicable to all voltage network systems worldwide. The IEEE journal publication by Kyei, Ayyanar, Heydt, Tallam and Belvins entited "The design of power acceptability curves" [8] discusses the CBEMA/ITIC curve and outlines its derivation.

2.2.2 Sag/Swell and Interruption Standards

The IEEE 1159 standard [9] categorises a wide range of electrical disturbances according to their typical duration and magnitude. Figure 2-4 summarises these categories:

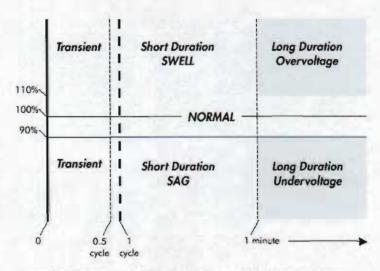


Figure 2-4 - Voltage Sags/Swells definition graph [9]

Sags and swells are described as short-duration variations; under and overvoltages are described as long-duration variations. When the voltage drops below 10 % of the nominal voltage, it is called an interruption.

The European electromagnetic compatibility standard relating to equipment voltage sag immunity is EN 61000-4-11:1994 Electromagnetic compatibility (EMC) -- Part 4: Testing and measurement techniques -- Section 11: Voltage dips, short interruptions and voltage variations immunity tests [38]. Further details on this standard are covered in the accompanying workbook.

The EMC standards define the disturbance limits and criteria that equipment should be manufactured to withstand. It also categorises various equipment and outlines test setups and procedures that should be applied to such equipment to assess their performance against the limit levels they define.

The voltage dip and interruption standard, EN 61000-4-11, defines test levels and durations which are shown in Table 2-2 and Table 2-3:

Test Level	Voltage Dips and Interruptions	Dur	ation
$\%~U_{ m T}$	% <i>U</i> _T	period	time
0	100	0.5	10ms
0	100	1	20ms
40	60	5	100ms
40	60	10	200ms
40	60	25	500ms
70	30	50	1000ms

Table 2-2 - EN 61000-4-11: Voltage Dips and Short Interruptions preferred test levels [38]

Voltage test level	Time for decreasing voltage	Time at reduced voltage	Time for increasing voltage
40 % U _T	2s ± 20 %	1s ± 20 %	2s ± 20 %
0 % U _T	2s ± 20 %	1s ± 20 %	2s ± 20 %

Table 2-3 - EN 61000-4-11: Timing of short term supply voltage variations [38]

The voltage dips and short interruptions are abrupt in nature and can start and stop at any phase angle on the mains voltage. The test levels to be used are expressed as a percentage of the rated voltage of the equipment and are stated as 0 %, 40 % and 70 % corresponding to dips and interruptions of 100 %, 60 %, and 30 %.

2.3 Voltage Transients and Surges

Transients are sudden 'spikes' on the supply voltage with various repetition frequencies and magnitudes. A surge is referred to as a single transient. Table 2-4 outlines the definitions, causes, effects and additional details relating to these disturbances.

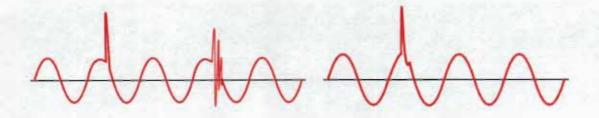


Figure 2-5 - Transients on the a.c. sinewave

Figure 2-6 - Voltage Surge

Definitions:	Transient: (also referred to as spikes, impulses or glitches) is a momentary sudden extreme rise in voltage (up to several thousand volts) over a very short time. These last for less than 1 ms. Transients are normally high frequency events with fast rise times.	
	Surge: another type of transient but is usually classified as one transient spike of longer duration. This results in a greater amount of energy transferred into the connected equipment. It therefore is more severe than transient impulses and increases the chance of damaging the circuits in a piece of equipment.	
Sources:	Lightning strikes, Utility line work/system faults, Inductive switching, Motors, Arc welders, Transfer switches, Power factor correction capacitors	
Effects:	In electronic equipment they can result in disruption or corrupted data and errors where data may be using the zero crossing rate as timing. If frequent equipment degradation and increased susceptibility to destruction is likely.	
Protection:	Power Conditioners and Surge Suppressors e.g. Transient Voltage Surge Suppressor (TVSS)	
Standards:	Transients: U.S: ANSI/IEEE Standard C62.41 Europe: EN 61000-4-4 Surges: U.S: ANSI/IEEE Standard C62.41 Europe: EN 61000-4-5	

Table 2-4 - Transients and Surges information

2.3.1 Transient Standards

The American standard governing transient overvoltage protection is ANSI/IEEE Standard C62.41 – 1991: Guide for Surge Voltages in Low Voltage AC Power Circuits [10]. This standard defines the transient environment that equipment may see and provides specific test waveforms that can be used for equipment withstand testing.

The European electromagnetic compatibility standard relating to equipments immunity to fast transient bursts is EN 61000-4-4:1995 (A1:2001) Electromagnetic compatibility (EMC) – Part4-4: testing and measurement techniques – Electrical fast transient/burst immunity tests [34]. Full details of this standard are covered in the accompanying workbook.

The test levels set out in the EN 61000-4-4 standard are shown in Table 2-5. They outline the transient withstand parameters for equipment of various uses which are categorised and explained in annex A of the standard.

Level	On Power Supply Port		On I/O signal, data & control ports	
	Voltage Peak kV	Repetition Rate kHz	Voltage Peak kV	Repetition Rate
1	0.5	5	0.25	5
2	1	5	0.5	5
3	2	5	1	5
4	4	2.5	2	5
x*	Special	Special	Special	Special

Table 2-5 - EN 61000-4-4: Burst Test Levels [39]

There has been some discussion recently regarding the content of this standard, which was originally published in 1984. As Harald Kunkle [11] explains, at the end of November 2002 an IEC technical group meeting was held to review comments on a new draft of the standard based on user inputs. A proposed change to the test levels is to include a higher repetition frequency of 100 kHz to bring it closer to a real event. The original 5 kHz and 2.5 kHz levels were based on very old generator designs that use

spark gaps as the high voltage switch to generate the fast transients. Most generators available today however are able to handle frequencies up to 1 MHz.

Section 6 of the standard details the transient burst test waveshapes as shown in Figure 2-7 and Figure 2-8.

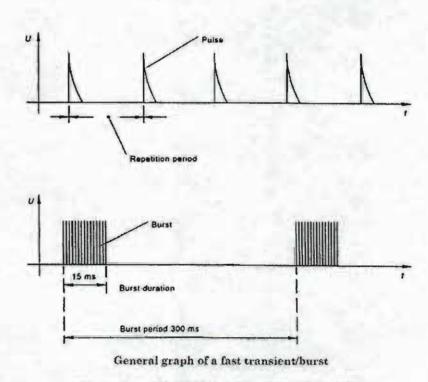


Figure 2-7 - EN 61000-4-4: Burst Waveform [39]

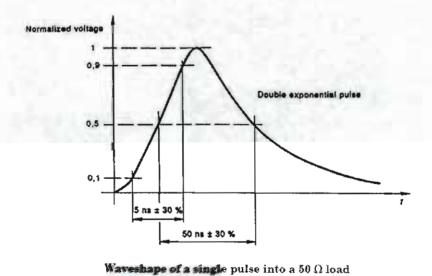


Figure 2-8 - EN 61000-4-4: Pulse waveform [39]

The test generator is required to produce these bursts, containing pulses occurring at a frequency of 5 kHz for 15 ms only and after a further 285 ms repeat the burst again and so on. A pulse within the burst is described as having a rise time of 5 ns and duration of 50 ns. They are also to be applied asynchronously, i.e. randomly on the input sine wave.

2.3.2 Surge Standards

As with transients the American ANSI/IEEE standard C62.41 applies in the USA.

In Europe the standard governing surge immunity is EN 61000-4-5:1995 (A1:2001) Electromagnetic compatibility (EMC) – Part4-5: testing and measurement techniques – Surge immunity test [40]. Full details on this standard are covered further in the accompanying workbook.

The EN 61000-4-5 standard defines the surge withstand level of the power supplies of interest here as being 2 kV (class 3 categorisation). Two surge generator specifications are discussed and described based on the surge waveform they produce. The Combination Wave (Hybrid) Generator (1.2/50 μ s – 8/20 μ s) is applicable to the equipment tested during this research. This generator delivers a 1.2/50 μ s (front time/time to half value) open-circuit voltage surge and an 8/20 μ s current surge into a short-circuit. These waveforms are shown in Figure 2-9 and Figure 2-10.

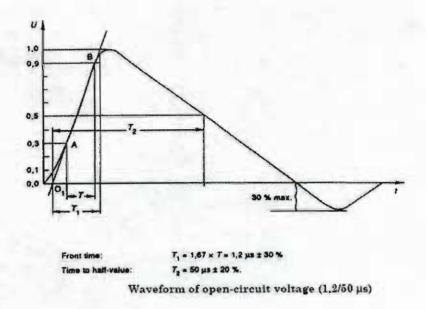


Figure 2-9 - EN 61000-4-5: 1.2/50 µs open-circuit voltage surge waveform [40]

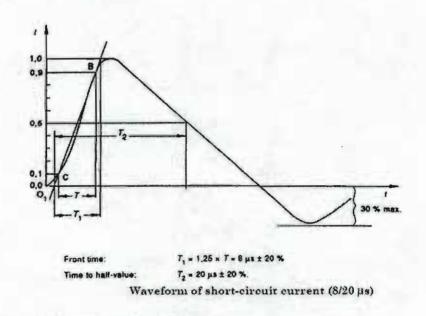


Figure 2-10 - EN 61000-4-5: 8/20 µs short-circuit current surge waveform [40]

They have become that standard waveforms to describe a lightning surge and as such using these test waveforms is said to be testing the lightning withstand of the equipment being tested (see section 7.2.1 for additional details on lightning surges).

Methods of coupling the surges onto the equipment are covered in section 6.3 of the standards text.

Section 8.2 of the standard describes how to apply the surge in the test. It states that the surges are to be applied line to line and line(s) to earth and to be synchronised at the zero-crossing and at positive and negative peak values of the a.c. voltage wave, i.e. at 0°, 90° and 270°.

2.4 Harmonic Distortion

Non-linear loads cause a distorted voltage waveform by absorbing electrical power at a different frequency to the 'fundamental' 50 Hz (60 Hz in the USA). Examples of such equipment include television and radio receivers and personal computers – all of which use switch-mode power supplies.

Fourier analysis allows the distorted waveform to be broken down into a set of sine waves with certain frequency and magnitude characteristics.

The distorted waveform repeats itself at the fundamental frequency, usually 50 Hz. Each successive sine wave, or harmonic, of this set has a frequency that is a multiple of the fundamental frequency. Hence, the 2nd harmonic has frequency 100 Hz, 3rd harmonic 150 Hz, 4th 200 Hz, and so on.

The magnitude characteristic, also called the *Harmonic Distortion Factor*, of each harmonic is represented as a percentage of the RMS value of the <u>fundamental</u>, not the total RMS of the distorted waveform.

The aggregate effect of all harmonics is called the 'Total Harmonic Distortion (THD)'

$$\%THD = \frac{\sum RMS \text{ of all Harmonics}}{RMS \text{ of Fundamental}} \times \frac{100}{1}$$

The "odd harmonics" (3rd, 5th, 7th, 9th, etc.) are symmetrical with respect to 90° whereas the "even harmonics" (2nd, 4th, 6th etc.) are asymmetrical with respect to 90°. This infers that, at 90°, the odd harmonics are at a positive or negative peak and even harmonics are at the zero crossing points.

Single-phase loads tend to generate the 3rd harmonic and three-phase loads generate the 5th and 7th harmonics. The 3rd harmonics influence is of more concern as it is difficult to filter out.

Harmonic No.	3	5	7	9	11	13	etc.
Phase	0	-	+	0	3 - 5	+	etc.
Sequence							

Table 2-6 - Sequence of the odd harmonics

The effects of the harmonics on the phase sequences are summarised as follows:

Sequence	Direction	Effects
+	forwards	Heating
	backwards	Heating and problems for motors
0		Heating and Accumulation in the
		Neutral Conductor

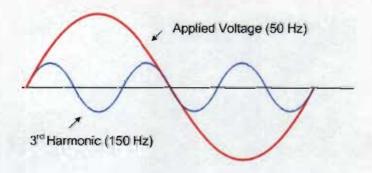


Figure 2-11 - Third Harmonic waveform

Figure 2-11 shows the fundamental and the 3rd harmonic. It can be seen that there are three cycles of the third harmonic for each single cycle of the fundamental.

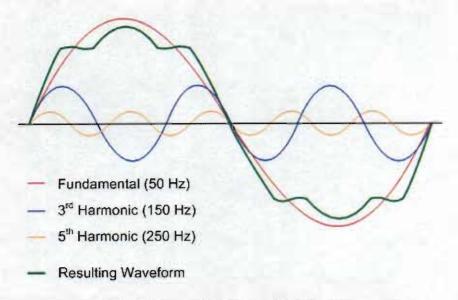


Figure 2-12 - Addition of Odd Harmonics

Figure 2-12 shows the affect the addition of the fundamental 50 Hz sine wave and the 3rd and 5th odd harmonics has on the resulting waveshape. The result is a non-sinusoidal distorted waveform.

Triplen Harmonics are harmonics beginning with the 3rd and multiples of three after that. These are of particular importance and cause the most problems on the electricity system. If there are balanced 50 Hz currents on all three phase conductors, the neutral current will add to zero. The 3rd harmonic of each of the three phase conductors is exactly in phase. When these zero-sequence triplen harmonic currents come together on the neutral, rather than cancel, they actually add up resulting in there being more current on the neutral conductor than on the phase conductors. This creates a risk of fire since the neutral is not protected by a fuse. Resizing of the neutral conductor to at least the same as the phase conductors needs to be done to compensate for this effect. This problem is particularly prevalent with single-phase electronics based loads.

Examples of equipment that generate triplen harmonics are: [12]

- Computers
- Office equipment
- Welding equipment
- Generators

- Rectifiers
- UPS
- Home electronic appliances

Power factor correction can also be incorporated into the design of these types of equipment to help limit the harmonics injected back into the system.

For a more detailed overview of harmonic distortion consult appendix A.3.

2.4.1 Harmonics Standards

Standards governing harmonics for utilities are listed in the *IEEE Standard 519*: Recommended Practice & Requirements for Harmonic Control in Electric Power Systems [13] and also in the European standard EN 50160:2000: Voltage characteristics of electricity supplied by public distribution systems [14].

Harmonic emission limits by equipment is outlined in EN 61000-3-2:2001 Electromagnetic compatibility (EMC) - Part 3-2: Limits - Limits for harmonic current emissions (equipment input current up to and including 16 A per phase) [15] and is discussed in full in the accompanying workbook.

EN 61000-3-4 [16] covers equipment that require greater then 16 A at the input.

The *IEC G.5/4* [17] standard is used within Europe as a "guidance as to the limits of harmonic distortion that may be fed into the electricity supply system by customers supplied from low or high voltage systems and to the limits of harmonic voltage distortion caused thereby." [18]

EN 61000-3-2 gives emission limits for harmonic currents injected into the public mains supply system from equipment having an input current up to and including 16 A per phase.

From the 1st January 2001, harmonic requirements became mandatory for most mains powered products. Amendment prA14, introduced for 1st January 2001, clarified issues relating to the classification of equipment. It redefined class D equipment (that which describes the power supplies of interest here) by application and not by the previous input current wave shape description. The limits however did not change in the amendment. The limits for class D equipment are presented in Table 2-7.

Limits for Class D equipment

Harmonic order	Maximum permissible harmonic current per watt mA/W	Maximum permissible harmonic current
3	3,4	2,30
5	1,9	1,14
7	1,0	0,77
9	0,5	0,40
11	0,35	0,33
$13 \le n \le 39$ (odd harmonics only)	3,85 n	See table 1

Table 2-7 - EN 61000-3-2: Harmonic Emission Limits for Class D equipment [37]

These limits are expressed in terms of the input power consumed by equipment and not using a fixed current value as is the case for the other classes described in the standard.

2.5 Conclusion

The most common types of disturbances known to affect low voltage domestic equipments are sags, swells, interruptions, fast transients and surges.

This chapter has defined all these terms and identified the relevant electromagnetic compatibility standards for the equipment being considered for this research. The test levels for proof of the conformity with the standards for each of the above disturbances have been extracted and explained.

These tests levels will form the test regimes to be used to establish conformity with the standard's limit levels of the equipment being considered. The testing of the equipment is discussed in detail in Chapter 5.

In addition this chapter also dealt with the effect of the appliances on the supply in terms of their harmonic emission levels and the associated harmonic standards.

As part of this research a check will be made to establish if the equipment being considered here is in conformity with the harmonic emission levels laid down in the appropriate standards. This is considered in Chapter 5.

Chapter 3 Computer Modelling Simulation Packages

3.1 Introduction

This chapter discusses the computer simulation packages commonly used for circuit simulations techniques used to further investigate the performance of switch-mode power supplies in the presence of supply disturbances. A model of a switch-mode power supply is developed and subjected to the EMC tests outlined in Chapter 5. Switch-mode power supplies are discussed in detail in the next chapter.

In addition the selection of the appropriate simulation software is discussed and comparisons made between the main software packages available.

It should be noted also that computer simulation is also used to investigate the behaviour of switching and lightning surges in medium voltage distribution networks and this is discussed separately in Chapter 7.

The selection of the appropriate software for both SMPS and network analysis is dealt with here.

3.2 Circuit Simulation Packages

In the past three decades there has been significant effort in developing digital simulation packages for use on personal computers, mainly due to increasing design complexity and finding cost cutting techniques. Also, since power systems are highly complex the behaviour of these systems is best studied through simulation.

There have been many papers published by academics and industrial engineers that illustrate studies into the various model analysis techniques. Numerous commercial simulation packages are available. The main simulation methods, state-variable analysis, nodal analysis and modified nodal analysis have been applied to different simulation packages, the most popular being *Electromagnetic Transients Program* (EMTP) for power system networks, *Simulation Program with Integrated Circuit Emphasis* (SPICE) for electronic circuits and power electronics, and more recently, MATLAB from Mathworks Inc.

These three computer packages were used during the course of this research and are described in the following sections.

3.2.1 EMTP Simulation Software

The origins of EMTP date back more than 20 years. The Electromagnetic Transient Program was originally developed by Professor Hermann W. Dommel in Germany, who brought the program to Bonneville Power Administration (BPA) in the late 1960's.

In 1982 the EMTP Development Coordination Group (DCG), a consortium of government agencies and utilities, was founded. In 1984 it joined forces with the Electrical Power Research Institute (EPRI) to enhance, maintain and develop the EMTP program. Version one of the software was released in 1987 and version two followed in mid 1989. The latest version available is EMTP96 released by the EPRI. This version provided a significant advance in the program. In previous versions huge amounts of code for every conceivable circuit element was generated and at times was rather unreliable. The EPRI group recoded and extended most parts of the program to improve its reliability and functionality. A graphical user interface (GUI) for the software was introduced by Ontario Hydro (now Hydro One Networks Inc.) which increased the user friendliness of the software significantly.

Other variants of the software, such as Alternative Transient Program (ATP) and Electromagnetic Transients for DC (EMTDC) have also been developed. All of the packages are based on the trapezoidal integration rule and the nodal approach and use fixed-step calculation algorithms, which have been proven to yield excellent results for power systems free of power electronic devices.

3.2.2 MATLAB – Power System Blockset Circuit Simulation Tool

MATLAB (Matrix Laboratory), developed by The Mathworks Inc., is an interactive computing environment of for numerical calculations and graphics. As its name suggests it is especially designed for matrix computations. It can be used for day-to-day computations with powerful mathematical functions and graphics. Matlab also can be

used for programming using script languages. Matlab's basic workspace can be further enhanced by the use of specialised toolboxes. The toolboxes relating closest to electrical engineering are the Control System Toolbox, Signal Processing Toolbox, Simulink and the Power System Blockset.

The Simulink component of MATLAB is a software package for modelling, simulating, and analyzing real world dynamic systems. It supports linear and nonlinear systems, modelled in continuous time, sampled time, or a hybrid of the two. For modelling, it provides a GUI for building models as block diagrams, using click-and-drag mouse operations. With this interface, one can draw the models just as they would with pencil and paper. Simulink extended Matlab's high-performance mathematics language to enable users to develop systems to tailor for certain applications.

Papers such as "SIMUPELS: Simulation of power electronic systems in the MATLAB-SIMULINK environment" [19] in 1995 by Gheorghe, Neacsu, Pittet, Yao and Rajagopalan and "Creating an electromagnetic transients program in MATLAB: MatEMTP" [20] in 1997 by Mahseredjian and Alvarado initially proposed using the power of MATLAB and Simulink to create a new design tool to redevelop the EMTP program in the MATLAB environment. Such thinking led to the creation of the *Power System Blockset (PSB)*.

The PSB was designed by the Power Systems Testing and Simulation Laboratory of Hydro-Quebec utility company. It uses the MATLAB/Simulink environment to represent common components and devices found in electrical power systems. By using Simulink the user can take advantage of a "click and drag" GUI thus enabling relatively easy construction of circuit topologies and interaction with other Simulink subsystems.

The Power System Blockset has since been renamed to *SimPowerSystems* in the recent release of version 6.5 (release 13) of MATLAB, It will however, within this thesis, continue to be referred to as its original name to maintain consistency with the work previously completed. The PSB main window is shown in Figure 3-1.

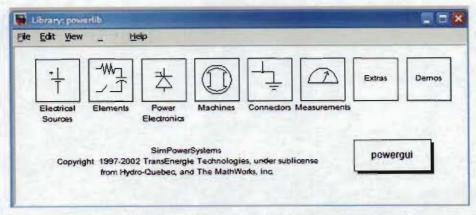


Figure 3-1 - The Power System Blockset Main Library Window

Each library block contains various circuit components that can be dragged to a workspace to create the desired power system model.

3.2.3 EMTP vs. Matlab Power System Blockset

Historically EMTP has been used for simulation work for power systems. It became widely used all over the world. Work discussed in past journal papers have mostly described the use of this program for simulations. Since the introduction of the Power System Blockset in Matlab in the late 1990's there has been a drift towards using this software package since it is far more user friendly, more comprehensive and easier to master. It also has the added flexibility of integration with the other powerful tools within the Matlab environment.

There have been many papers published addressing the introduction of the PSB [21] and also assessing its performance with comparisons to EMTP and other simulation software tools. Publications such as "A comparison between three tools for electrical transient computations" [22] by Schavemaker, de Lange and van der Sluis and "A link between EMTP and MATLAB for user-defined modelling" [23] discuss these two simulation packages and present example simulations where the results are compared.

Simulation of the example circuit model illustrated in the paper by Schavemaker shows, the processing time using the PSB is significantly greater than that when EMTP is used (however when the first PSB simulation is run the state-space computation of the circuit takes 8 seconds, a couple of seconds more than EMTP but in subsequent runs this processing is skipped and the computation times reduce to 0.5 seconds).

The authors of [22] present a comparison table, as shown in Table 3-1, outlining their views on the two packages. They conclude that for larger simulations using many elements EMTP is "the best solution" and that "MATLAB is unbeatable where programming freedom and flexibility is concerned." They also advise the use of the PSB for dedicated studies and when circuit computations are embedded in software.

	EMTP96	MATLAB PSB
User-friendliness	*	V/x
Computational speed	√/×	V
Variable step-size	×	/
Multiple numerical integration routines	×	~
Flexibility	×	/
Creation of new models	×	√/x
Number of circuit element models	✓	×
Export Functionality	√	1

Table 3-1 - General comparison between EMTP and MATLAB PSB [22]

Because it was historically the most widely used program the ATP package was obtained and installed. From the very start the package presented numerous problems and complications. It installed incorrectly and eventually the settings needed to rectify this were found and corrected. As explained previously the package is made up of a number of software components and requires some study to configure them to interact. Overall the program proved to be highly frustrating and not user-friendly. It was clear that it would take a long time to get to grips with this software. Considering time constraints and the industries trend turning towards using the Power System Blockset attention was turned to using it instead.

(Note: there is a new totally revamped version of EMTP, called EMTP-RV coming out soon. It is the end result of an "EMTP restructuring project" undertaken in 1998 by the DCG and promises a completely new graphical interface making it far more user-friendly. The computational engine has also been totally redesigned from scratch. From the initial information on the website [24] it appears that this new version is going to be

extremely user friendly and easy to use and a lot more powerful than before, even more so than the PSB).

3.2.4 PSpice Circuit Simulation software

Developed in the mid-1970s by the University of California, Berkeley, the primary aim of the SPICE program (initially named CANCER) was to aid design in the electronics industry, especially integrated circuit designers. It is a general-purpose circuit simulation program conceived to speed up the design phases of equipment being developed. Through private investors the SPICE architecture has evolved into many packages.

One such package is *PSpice* (a commercial version of SPICE developed by Microsim and now maintained by Orcad) which has become the most popular version of SPICE.

In addition to the basic circuit elements R, L, C, independent and controlled sources etc., models for transmission lines and the most common semiconductor devices are available. It is mainly used to simulate electronic and electrical circuits for d.c., a.c., transient, zero pole, distortion and noise analysis. SPICE uses the nodal approach with variable-time-step integration algorithms which enables calculation of power electronic circuits incorporating switching.

SPICE is capable of performing non-linear d.c., non-linear transient and linear small-signal a.c. circuit analysis. The transient analysis is probably the most important analysis type. It computes the voltages and currents in a circuit with respect to time and is most meaningful when time-varying input signals are applied to the circuit.

The basic SPICE input and output interfaces are through text files where the input file would contain a nodal description of the circuit and the output file would contain the numerical results of the simulation.

SPICE however is not particularly suited to power systems analysis as, unlike the PSB, it does not contain the specific models needed. This means that these electrical machines, drives, circuit breakers etc. would need to be constructed using the basic elements mentioned and would be very time consuming.

The PSpice package contains a number of different applications. The main application is called *PSpice A/D*. Here the results of the simulations are displayed. The input .cir files and output files can also be constructed and edited. The simulation resulting waveforms are called using the .PROBE statement in the circuit input file. By "adding traces" to the probe window, voltages and current at the nodes in the circuit can be displayed.

The *Schematics* program enables the user to create schematic drawings of their circuits. It creates a user friendly interface for the PSpice package and calls PSpice A/D probe to display the results of the simulation.

Orcad Capture is used to create more complex design projects. Like 'schematics' is has its own circuit schematic creation program and can combine numerous schematics within a design. It also calls PSpice A/D probe to display simulation results.

3.2.5 PSpice vs. Matlab Power System Blockset

With the introduction of the Power System Blockset software it is obvious that there would be comparisons made between it and other established simulation tools in use. Publications such as "MATLAB/Simulink and PSpice as modelling tools for power systems and power electronics" by Le-Huy and Sybille [25] and "A power system simulation tool based on Simulink" by Dessaint, Al-Haddad, Le-Huy, Sybille and Brunelle [26] provides descriptions and simulations using each tool and the results are compared. The former concludes that the Power System Blockset is "well suited to the simulation of medium size power systems and power electronics using variable or fixed step algorithms from Simulink." PSpice is well suited for device-level modelling of small size systems (power converters, transformer transients etc.) and for larger size power systems the simulation times are said to be excessive.

[26] illustrates the simulation of an a.c.-to-d.c. resonant converter in both Matlab PSB and PSpice. The results obtained illustrated that the PSB showed very good agreement with the results from PSpice. It also concludes that the PSB is well suited for the simulation of electric circuits containing switching devices and the PSB has the

advantage of containing power electronics and electric machinery libraries that are suited to simulating power systems and drives.

Chapter 4 Switch Mode Power Supplies

4.1 Introduction

The research scope required an investigation into low voltage residential domestic appliances as opposed to medium voltage industrial environments, which is a growing area of discussion in terms of power quality. From this it followed that domestic appliances were to be EMC tested to the standard limits in order to assess if they are performing according to the appropriate standards. From subsequent research on domestic appliances it was clear that most of them featured the same power supply technology – switch-mode power supplies. Since this is the first point of entry into the appliance it was decided to obtain sample power supplies from appliances that most claims were made against. Therefore research into switch-mode power supply technology was essential to gain an understanding of their operation and design. The following sections describe the technology used in these power supply designs.

4.2 Switch-Mode Power Supply Circuit Operation

The switch-mode power supply (SMPS) uses high frequency switching devices (most commonly Bipolar Junction Transistors (BJTs) or MOSFET transistors) with varying duty cycle to maintain an output voltage. The most significant differences between linear and switch mode regulators involves their efficiency, size, weight, thermal requirement, response time and noise characteristics. The advantage of the switch-mode power supply is that the switching device, in either on or off state, dissipates very minimal power loss, which leads to high efficiency. Since it can operate at very high frequencies, a smaller transformer using ferrite cores can be used. Much smaller capacitors can be used than in linear power supplies since the rectified mains voltage is chopped and the energy storage for hold-up can be accomplished on the primary side of the transformer.

The switching mode technique does however have its own disadvantages. This design is considerably more complex. The control circuitry controlling the switching in the supply is much more complex than its linear counterpart. In addition, there is increased

noise present at both the input and the output as a result of the high frequency switching. The output voltage contains switching noise which must be removed. An L-C filter is usually incorporated at the output stage (forward-mode converter) to filter out this noise.

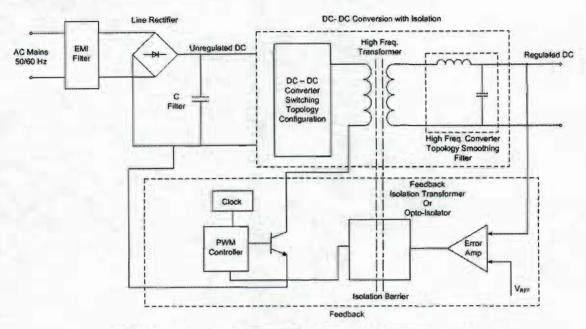


Figure 4-1 - Schematic Circuit of a Switch-Mode Power Supply

Figure 4-1 above shows a simple schematic of switch-mode power supply.

There is usually a selector switch on the a.c. supply side to cater for the 230 Vac mains of most of the world and the 115 Vac mains level of America. There are also power supplies available that can auto select the correct voltage range. These are known as universal power supplies and can suffer from the problem of auto switching to the wrong input selection if the input voltage is significantly reduced. For instance, when operating a universal type supply on a 230 V system and the voltage has dipped to around 170 V the supply could auto switch between the 100 - 120 V and 200 - 240 V input levels and confusion could lead to the former range being selected and as a result damage the supply.

The input to the supply may also include electromagnetic interference (EMI) or surge protection. An input line fuse is also present.

A diode bridge rectifier and large filter capacitor is used to rectify the a.c. line input to an unregulated d.c. level usually in the range 160 - 320 V. The smoothing capacitor is

charged (thus drawing current) only during the peak of the mains voltage waveform. A d.c. voltage is then seen across the switching transistor circuitry and the transformer.

The switching circuit can be configured in numerous ways, see section 4.3.5 for more.

When the transistor is on, current increases linearly in the primary of the transformer (based on the voltage applied and the leakage inductance of the primary winding). Little power is transferred to the secondary during this phase of the cycle. When the transistor is off, the field in the transformer collapses and power is transferred to its output. The longer the transistor is on, the more energy is stored (until saturation), hence controlling the length of time the transistor is on will determine the amount of power available on the output.

The output is monitored by a reference circuit on the main output. (Note: if the power supply transformer provides multiple outputs, only one main output is monitored and hence regulated). This feedback circuit controls the duty cycle of the switching device as well as incorporating various overload and overcurrent protection circuitry. The duty cycle is effectively the amount of time the transistor is operating in the on state. By varying the duty cycle of the switching device the output voltage can be maintained at a constant desired value.

Many switch-mode power supplies use 'opto-isolators' in the feedback circuit. An opto-isolator is an LED (light emitting diode) and a photodiode in a single package which provides an isolation barrier between the low voltage transformer secondary outputs and the mains connected primary (if required). A reference circuit on the output side senses the main output voltage and turns on the LED of the opto-isolator when the output voltage exceeds the desired value. The photodiode detects the light from the LED and causes the pulse width modulator to alter the pulse width of the switching waveform (the duty cycle) in order to alter the amount of output power from the transformer to maintain a constant output level. An alternative design is to use small pulse transformers in place of the opto-isolator to provide the isolated feedback.

The internal switching frequency of these power supplies can range between 20 kHz and 100 kHz, ensuring operation above the human range of hearing.

The d.c.-d.c. high frequency conversion rectifier stage defines what type of power supply unit it is. It can be designed to give a desired higher or lower d.c. output level or multiple various d.c. output levels. The conversion technology used at this stage is described in more detail in the next section.

To clarify, the term *switch-mode regulator* is used to describe a circuit that adopts feedback to maintain a constant d.c. output voltage.

The term *switch-mode converter* is used to describe a circuit that simply takes a d.c. input and provides single or multiple d.c. outputs.

A switch-mode power supply is essentially a switch-mode regulator but includes additional circuitry for overvoltage and overcurrent protection as well as other control circuitry. It also adds an input a.c. to d.c. (unregulated) rectification stage to the regulator input as explained previously.

4.3 DC - to - DC Converter Topologies and Theory

There are two basic types of switch-mode converters, Forward Converters and Flyback Converters. The basic configurations associated with these two types are the Buck Converter and the Boost Converter respectively. There is also a third configuration which is a combination of the two converters called the Buck-Boost Converter.

Many popular topologies are derived from the buck type converter, such as the pushpull, the full-bridge and half-bridge.

4.3.1 Forward-mode Converter - The Buck Converter

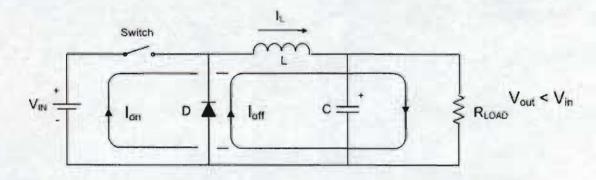


Figure 4-2 - Buck Converter

The buck converter, Figure 4-2, (or forward-mode converter, or voltage step-down/current step-up converter – the buck converter has many names) accounts for 80 to 90 % of all converters sold. Understanding this is essential to understanding switch-mode power supplies. It is most recognised by the L-C low-pass filter on the output which is incorporated to smooth the pulsating wave on the output from the switch.

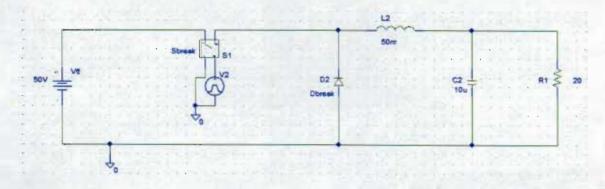


Figure 4-3 - PSpice Schematics Buck Converter Circuit

Figure 4-3 shows the buck converter implemented in the circuit simulation package 'PSpice' (see section 3.2.4 for details) and simulation waveforms obtained are shown in Figure 4-4. The circuit is supplied with 50 V_{dc} , the switching frequency is 30 kHz and the duty cycle ratio of the switch is set to 50 %.

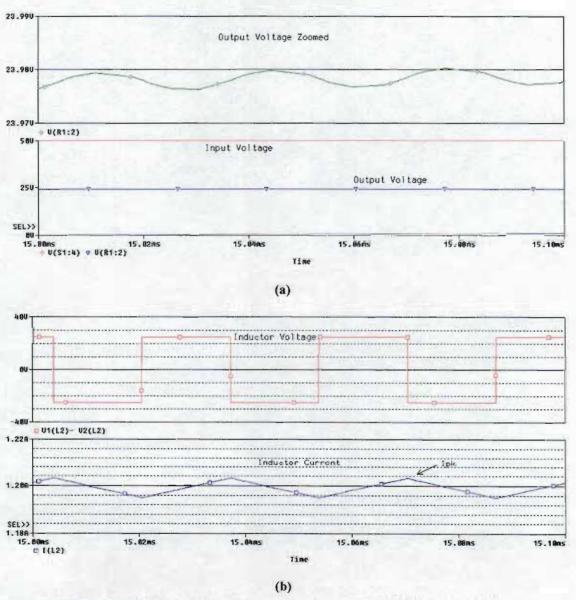


Figure 4-4 - Buck Converter PSpice waveforms with duty cycle ratio at 50 % Input and Output (also zoomed) voltages

(b) Inductor voltage and current as the switch is on and off

The operation of the circuit can be broken into two periods – when the switch is in the on position and the off position. The "duty cycle," D, of the switch is given by:

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T} = t_{on} f$$
 (4-1)

where f is the switching frequency in hertz. Steady-state operation is assumed.

Switch on: When the switch is on (closed) the energy from the input voltage source flows directly into the L-C filter. And during steady-state operation an output voltage will appear on the output of the converter. The current through the inductor rises linearly from an initial current given by the remaining flux in the inductor.

With the switch closed for time DT, the inductor current during this 'on' state is given by:

$$I_{L(on)} = \left(\frac{V_{in} - V_{out}}{L}\right) DT + I_{\min}$$
(4-2)

Switch off: Energy is built up as magnetic flux in the core of the inductor during the on state. When the switch opens - changes to off (at I_{pk}) - this energy is released and supplies the load. The diode becomes forward biased and provides a return path for the current enabling it to flow to the load. The initial current for the 'off' period of operation is the maximum the current reached in the 'on' position at the point the operation state changed, which is I_{pk} in the waveform. The switch is open for time (1-D)T. Therefore the decreasing inductor current is given by:

$$I_{L(off)} = I_{pk} - \left(\frac{V_{out}}{L}\right)(1-D)T$$
(4-3)

This continues until a controller changes the state back to 'on'.

The waveforms show the buck converter circuit operating in *continuous mode* i.e. the inductor current remains positive throughout the switching period. *Discontinuous* operation is conversely characterised by the inductor current returning to zero.

Further calculation of these current formulae under steady state reveals the output voltage to be

$$V_{out} = V_m D ag{4-4}$$

By choosing appropriate values of L and C the buck converter can be optimised to produce a steady, near ripple free DC output voltage. A rule of thumb when choosing

the inductor and capacitor values is to start with an inductor value that results in a peak-to-peak inductor current that is 10% of the full load current. Therefore knowing the input and output voltage, the load current and the switching frequency, a value for the inductor can be ascertained from the basic equation, $V = L(d^i/dt)$.

Note: the minimum value for the inductor for continuous current mode can be quickly calculated using the following formula since the boundary between continuous and discontinuous operation is $I_{min} = 0$ and the desired switching frequency is established:

$$L_{\min} = \frac{(1-D)R}{2f}$$
 (4-5)

The capacitor is used to decrease as much as possible the output ripple voltage, so carefully choosing a correct capacitor value will yield a near constant d.c. output.

As explained in the power supply design guide from Jerrold Foutz [27], the capacitor value can be calculated firstly by considering overshoot and applying another rule of thumb. This being, making the characteristic impedance of the filter, Zo, equal to the load resistor. Solving $Zo = \sqrt{\frac{L}{C}}$ will yield a value for C.

Having obtained values of inductance and capacitance the output ripple can be determined.

4.3.2 Flyback-mode Converter - The Boost Converter

The boost converter (or step-up converter), shown in Figure 4-5, has the same operation principles (and components, but configured differently) as the buck converter but is designed to give an output voltage that is higher than the input. As well as being used in regulated d.c. power supplies it is also used for regenerative braking in d.c. motors.

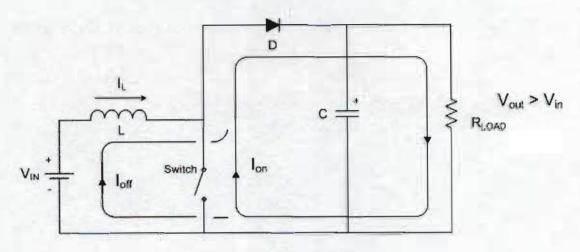


Figure 4-5 - Boost Converter

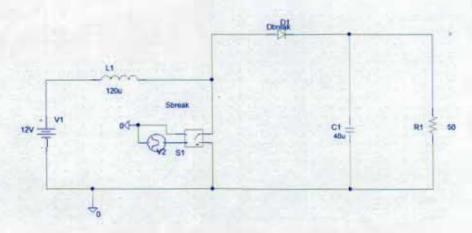


Figure 4-6 - PSpice Schematics Boost Converter Circuit

Figure 4-6 shows the boost convert implemented in the PSpice schematics program and Figure 4-7 shows the simulation waveforms results of this circuit. The circuit specification is a 12 V input, switching frequency of 25 kHz and duty cycle ratio of 60 %. It gives an output of 27 V.

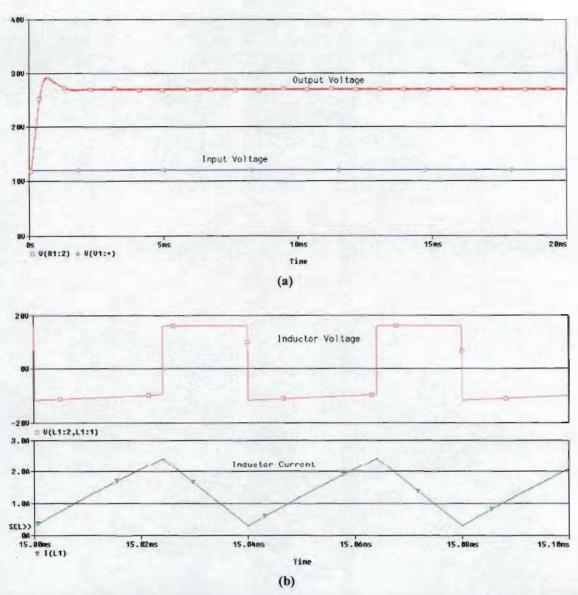


Figure 4-7 - Boost Converter PSpice waveforms with duty cycle ratio at 60 %

(a) Input and Output voltages

(b) Inductor voltage and current as the switch is on and off

Again analysis is best achieved considering the on (closed) and off (open) positions of the switch.

When the switch is closed the diode is reversed-biased. V_{in} supplies the inductor with energy and the current increases linearly, the change in inductor current is given by

$$\Delta I_{L(on)} = \frac{V_m DT}{L} \tag{4-6}$$

When the switch is opened, the inductor current cannot change instantly so the diode becomes forward-biased and provides a path for the inductor current. The output receives energy from both the inductor and V_{in} . So assuming steady-state operation and

constant output voltage, achieved if the filter capacitor is very large, the change in inductor current is

$$\Delta I_{L(off)} = \frac{(V_{in} - V_{out})}{L} (1 - D)T$$
 (4-7)

Under steady-state the inductor current at the end of this switching cycle must be the same as that at the beginning, thus

$$\Delta I_{L(on)} + \Delta I_{L(off)} = 0 \tag{4-8}$$

Further calculations yield the output voltage to be

$$V_{out} = \frac{V_{in}}{1 - D} \tag{4-9}$$

and the minimum inductor value to be derived from

$$L_{\min} = \frac{D(1-D)^2 R_{LOAD}}{2f}$$
 (4-10)

Also,

$$P = \frac{V_{out}^2}{R} \implies I_L = \frac{V_{in}}{(1-D)^2 R}$$
 (4-11)

$$I_{\text{max}} = I_L + \frac{\Delta I_{L(on)}}{2} : I_{\text{min}} = I_L - \frac{\Delta I_{L(on)}}{2} = 0$$
 (4-12)

The output ripple voltage formula is

$$\frac{\Delta V_o}{V_o} = \frac{D}{RCf} \tag{4-13}$$

From these formulae, inductor and capacitor values for the output filter can be calculated.

The boost inductor must store enough energy to supply the output load for the entire switching period, $t_{on} + t_{off}$. They are usually limited to a 50 % duty cycle to ensure there is a time period for the inductor to deplete itself of its energy.

Replacing the inductor with a transformer results in an isolated flyback converter, which can step-up or step-down the voltage. This is discussed later in this chapter.

4.3.3 The Buck-Boost Converter

The Buck-Boost Converter (see Figure 4-8) is a cascade connection of the buck converter and the boost converter and can also be called a voltage inverter because its output is opposite in polarity to the input. It is used to achieve opposite polarity output voltages that are either higher or lower than the input. If the duty cycle is greater than 50 % it functions as a step-up converter and if the duty cycle is less than 50 % it functions as a step-down converter.

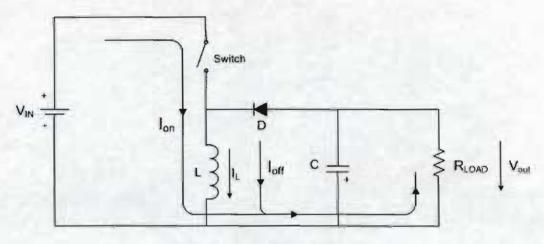


Figure 4-8 - Buck-Boost Converter

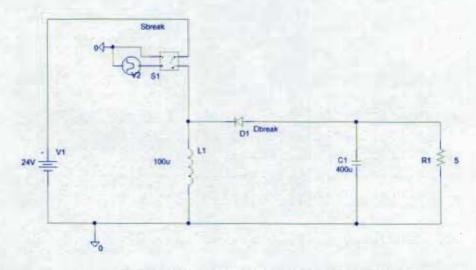


Figure 4-9 - PSpice Schematics Buck-Boost Converter Circuit

Figure 4-10 shows an example waveform of the buck-boost circuit simulated in PSpice (see Figure 4-9). The converter was configured to produce a negative 12 V output from a 24 V input. The switching frequency was set at 25 kHz and a duty cycle of 0.4 was implemented.

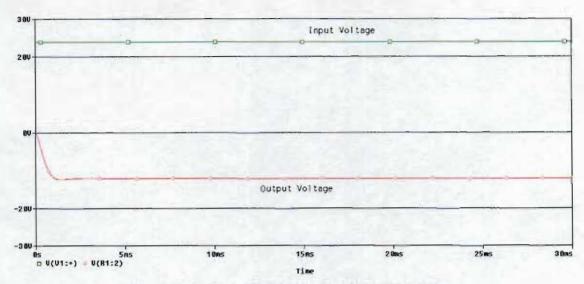


Figure 4-10 - Buck-Boost PSpice Simulation Waveforms

As the same calculations, illustrated previously, can be applied to the buck-boost converter, they will not be described again here.

4.3.4 The Cuk Converter

Another forward converter, the Ćuk converter (so named after its inventor Dr. Slodoban Ćuk, a leading researcher in SMPS technology) has been developed. It is similar to the buck-boost converter as it also provides a negative higher or lower output with respect to the input. Both the input and output circuits contain inductors, as shown in Figure 4-11, thus neither the input nor output current is pulsating. This greatly reduces conducted electromagnetic interference problems, allowing smaller filtering components. This is a significant drawback of the buck-boost. The Ćuk converter uses a capacitor for energy transfer as opposed to the inductor used in the previous topologies. The inductor L₁ acts as a filter to prevent large harmonic content. C₁ is the capacitor used to transfer energy to the load in the way inductors did before.

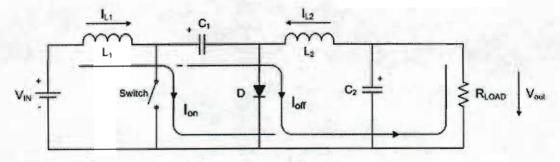


Figure 4-11 - Ćuk Converter

4.3.5 The Flyback Converter

The previous converter configurations discussed can be reconfigured to provide output isolation using an isolation transformer. They can also be configured to, by use of multiple secondary winding tap-offs, provide multiple d.c. output voltages.

The flyback converter, shown in Figure 4-12, is used in higher voltage, low current or low power applications where high output ripple can be tolerated.

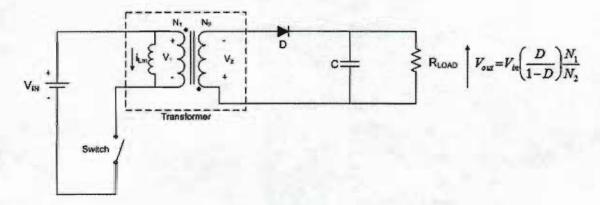


Figure 4-12 - Flyback Converter

When the transistor circuit switch is on magnetising energy is stored in the transformer, shown here as the magnetising inductance, i_{Lm} . With the switch on $V_I = V_{in}$ and the secondary current is zero which means the primary current is also zero since the diode is off. Hence the capacitor provides the load current.

When the transistor circuit switch is turned off, since current cannot change instantaneously in an inductance, the conduction path is through the undotted primary terminal of the transformer and the undotted terminal on the secondary site. This turns on the diode and the transformer secondary provides charging current to the capacitor and load current to R_{LOAD} . Hence, $V_1 = -V_{out} \frac{N_1}{N_2}$ and $V_2 = -V_{out}$.

Figure 4-13 shows waveforms obtained when the flyback converter is simulated in PSpice. The circuit implemented features a 30 kHz switching frequency with a duty cycle of 40 % and transformer turns ratio of 1:2. This gives an isolated approximate 8.5 V output from a 24 V d.c. source.

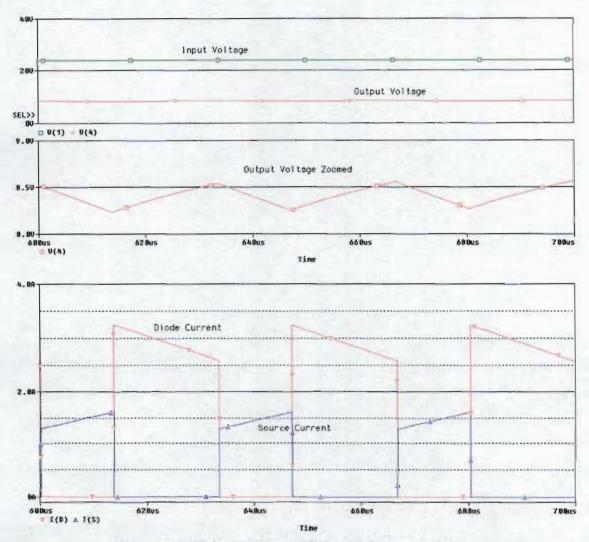


Figure 4-13 - Flyback converter PSpice simulation waveforms

The flyback converter is a simple circuit to implement as it has a low component count. It is highly popular in low-power applications. Its main disadvantage is that as the power requirements increase the transformer size also increases and the voltage stress (2V_{in}) across the transistor switch increases. They are typically used for applications up to 150 W.

4.3.6 The Push-Pull Converter

The push-pull converter, shown in Figure 4-14, has transformer isolation and uses multiple switches. A centre-tapped secondary is used, which results in only one diode voltage drop on the secondary side.

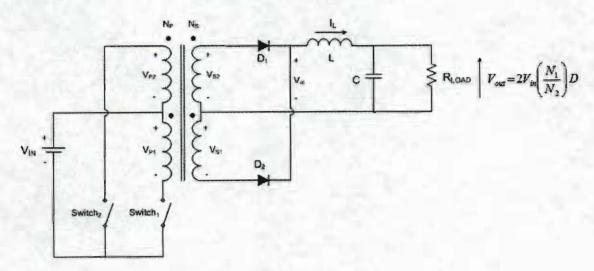


Figure 4-14 - Push-Pull Converter

Switch 1 on: When switch 1 is closed V_{in} is seen across primary winding P_1 . This voltage is transformed to the other three windings and diode D_1 is forward biased whilst diode D_2 is reverse biased. [28]

$$V_{P1} = V_{in} = V_{P2} (4-14)$$

$$V_{S1} = V_{in} \left(\frac{N_S}{N_P} \right) = V_{S2}$$
 (4-15)

$$\therefore V_L = V_{oi} - V_{out} = V_{S2} - V_{out} = V_{in} \left(\frac{N_S}{N_p}\right) - V_{out}$$
 (4-16)

Switch 2 on: $-V_{in}$ is seen across V_{P2} and V_{P1} . Diode D_2 becomes forward biased and D_1 is reversed biased. The energy from the transformer flux collapses and is coupled to the output. $V_{oi} = -V_{S2}$ and V_L calculates to the same positive pulse expression as above.

Both switches off: When both of the switches are open there is no current in the primary windings. D₁ and D₂ both become forward biased and the inductor current divides evenly between the two secondary windings.

$$V_{oi} = 0 \qquad \therefore \qquad V_L = -V_{out} \tag{4-17}$$

Further calculation (inductor current change during each switch state – not described here) yields the output voltage expression to be

$$V_{out} = 2 V_m \left(\frac{N_s}{N_p}\right) D \tag{4-18}$$

The PSpice simulated waveforms show the operation of the push-pull converter.

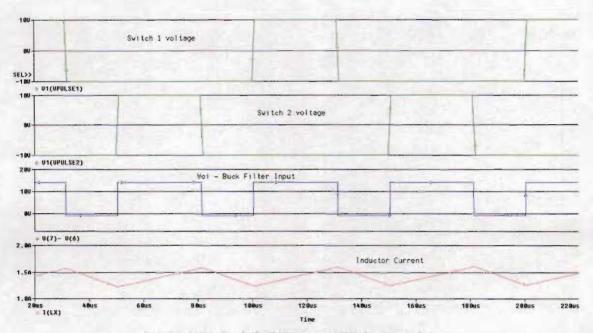


Figure 4-15 - Push-Pull Converter PSpice Waveforms

As can be seen, the voltage, V_{oi} , rectified by the diode is a positive pulsed waveform and is smoothed to obtain a near flat d.c. output by the buck filter before the load.

The push-pull converter is used in medium power applications. A small transformer core is used since it is excited in both directions. High transistor voltage stress is also an issue as with the flyback converter.

There are additional converter configurations but they will not be covered further here as only the main topologies are necessary.

4.3.7 Control of Switching Converters

The converters mentioned previously take a d.c. input and provide a different d.c. output. This is adequate provided the input voltage and the load never varies. Once either of these alter, the output voltage will be adjusted accordingly with the change. More often than not it is necessary to have a constant output value even when there are load variations or variations at the input. Therefore the converter needs to be adjusted to compensate for output differences. This is achieved through feedback, and using additional circuitry the transistor switching times can be altered to maintain the desired output since the output is a function of the input and the switching duty cycle ratio. (see Figure 4-16).

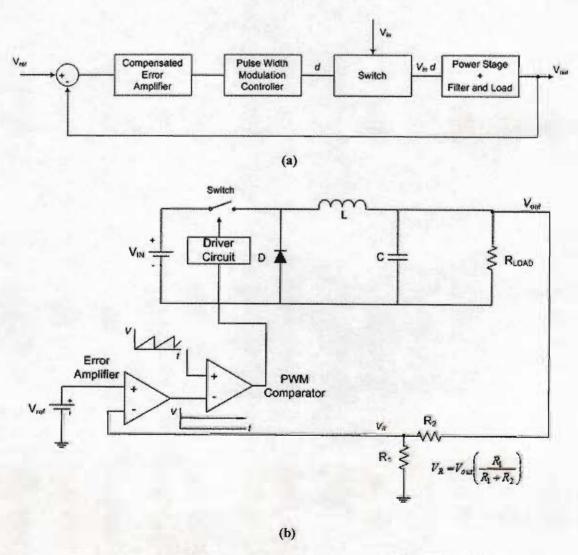


Figure 4-16 - Feedback Control Regulation of Switch-Mode Power Supplies

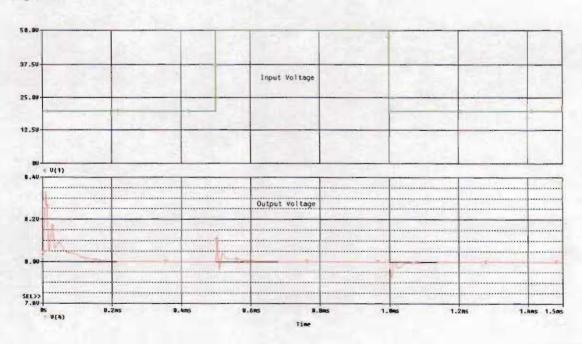
(a) Control structure diagram (b) Feedback compensation in a Buck converter

The output of the power supply, through negative feedback, is compared with a reference voltage, V_{ref} . The error amplifier produces an error signal which is sent to the Pulse Width Modulation (PWM) Controller which adjusts the switching times of the power supply.

The PWM circuit converts the output signal from the compensated error amplifier to a duty cycle ratio signal. A pulse width comparator compares a sawtooth waveform with the error amplifier signal. The output of the PWM is high when the error signal is greater than the sawtooth waveform value and the output is zero when the error signal is below that of the sawtooth.

If the output voltage falls below V_{ref} , the error amplifier output increases which in turn results in an increase in the duty cycle. Equally, if the output rises, the duty cycle ratio is decreased.

Figure 4-17 shows the response of a buck converter with output feedback compensation to a step increase in the input voltage simulated in PSpice. The input voltage increases from 20 V to 50 V after 5 ms for 5 ms. The output voltage response is also shown as well as the decrease in the duty cycle ratio from the PWM and the inductor current response.



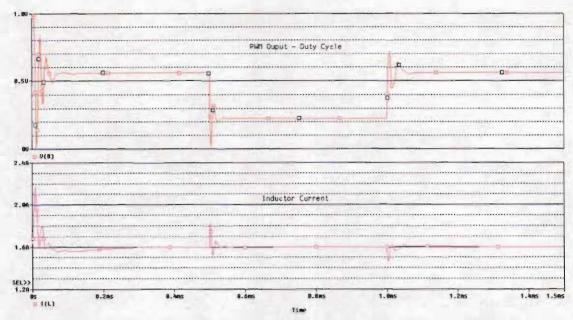


Figure 4-17 - Buck Converter Output Regulation response to input voltage increase

Figure 4-18 shows the same circuit in PSpice but this time the output load is doubled after 5 ms and returned to its previous state 5 ms later.

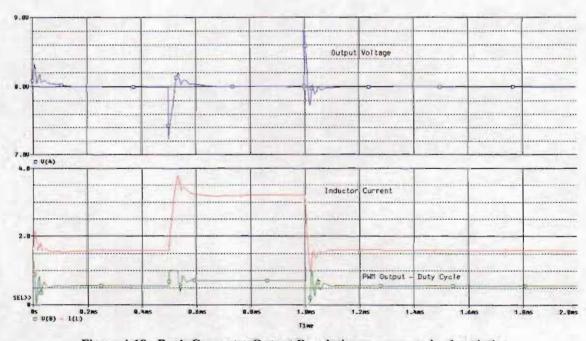


Figure 4-18 - Buck Converter Output Regulation response to load variation

As can been seen in the waveforms the duty cycle of the switching circuit is altered to maintain the output of the converter. In the case where the input voltage increased, in response the duty cycle decreases in order to keep the output regulated at 8 V, whereas when the load increased the duty cycle increased to achieve the same result.

Regulation of the output is essential for the internal circuitry within an appliance. They expect a certain voltage and can be damaged and/or malfunction if not supplied with the correct voltage level.

For power supplies with multiple output converters only a main output is regulated, not every output as this would increase the bulk and component count of the power supply. This is acceptable since the outputs are fed off the same transformer and will follow the same duty cycle ratio.

4.4 Personal Computer Power Supplies

The main task of the power supply in a computer is to convert the a.c. mains input into a useable d.c. voltage for the components inside the personal computer chassis. It can also provide protection for the internal circuit components of the computer and is essential to maintaining the stability of the computer system.

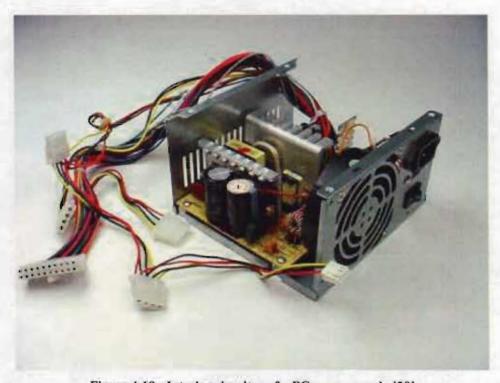


Figure 4-19 - Interior circuitry of a PC power supply [29]

Like almost every other appliance a computer is run internally using d.c. voltages and therefore (as with the other appliances) the computer power supply utilises switching technology to convert the mains a.c. to d.c. It is effectively a switch-mode power supply and is in itself classified as a "component" of the overall computer.

The computer power supply does have some additional circuitry over the switch-mode power supplies explained previously. For example, they can incorporate power factor correction circuitry. The power factor of traditional power supplies is about 0.6 to 0.7 but newer PC power supplies, especially larger ones for servers, have a power factor near to unity. This therefore makes the sizing of Uninterruptible Power Supplies (UPS's) easier and improves harmonic emission levels.

The term form factor describes a computer systems design in terms of general shape and dimensions and connections. Power supplies have to be built to accommodate these form factor specifications in order to fit into the PC chassis and connect correctly to the motherboard it is to provide power to. [30]

Personal computer power supply form factors (e.g. ATX and LPX) and the various output connectors and signals are detailed in appendix C. Refer to this for explanations of the terms used in relation to computer power supplies.

4.4.1 Power Supply Circuitry

All computer power supplies use switching technology. As mentioned previously the efficiency, reduced size and lighter weight advantages of switch-mode power supplies are essential for personal computers.

PC power supply schematics proved relatively hard to source, however Figure 4-20 shows a modern 200 W PC ATX power supply schematic diagram. This power supply schematic was drawn by Pavel Ruzicka. [31]

This circuit uses a push-pull transistor configuration circuit with output voltage regulation.

The input a.c. voltage passes through an input filter circuit to a bridge rectifier. The rectifier acts as a voltage doubler when the input voltage selector switch is set at 115 V. The varistors Z1 and Z2 provide overvoltage protection on the line input. Capacitors C5 and C6 filter the output of the rectifier to an un-regulated d.c. voltage of about 300 V. Resistors R2 and R3 are there to discharge the capacitors residual voltage after the power supply is turned off.

From here the secondary power supply circuitry is taken in order to supply the motherboard with the +5 V standby always on signal (discussed previously). Q12 controls the voltage and the voltage level on the secondary side of transformer T6 is regulated by the positive voltage regulator IC LM8L05 to the required 5 V.

An unstable voltage is taken off T6 through D30 to the main control IC1 (TL494) and to the control transistors Q3 and Q4. The +12 V and -12 V outputs are monitored by feedback through diode D.

The TL494 is a switch-mode power supply controller IC from Fairchild Semiconductor. It is used as the control circuit of the PWM switching regulator.

When in stand-by mode, i.e. power supply off, the power supply is blocked from operating by a positive 5 V voltage on the PS_ON (Power ON) pin through resistor R23 from the secondary power supply. Because of this voltage present transistor Q10 is off hence Q1 is also off which as a result applies a reference voltage of +5 V from pin fourteen to pin four of IC1. The switching circuit is now totally blocked. Transistors Q3 and Q4 are both off and the winding of transformer T2 is short-circuited. Due to this short-circuit there is no voltage on the power circuit section. The voltage on pin 4 of IC1 can be used to drive the maximum pulse width on its output. If PS_ON is at 0 V then the pulse width is at maximum and when it is at +5 V the pulse disappears. The PS_ON signal is also used by the 'Power Good' circuit to inform the motherboard to start operating, which occurs when the power good signal is set to +5 V (logic one).

When the power button is activated on a computer, the mother board logic circuits, fed from the +5 V standby signal, set PS_ON to ground. Transistor Q10 turns on and thus Q1 turns on. Capacitor C15 begins charging through R15 and the voltage on pin 4 of IC1 begins to decrease to zero thanks to R17. There is now maximum pulse-width and the power supply operates.

When the power supply is operating normally it is controlled by IC1. When power transistors Q1 and Q2 in the power circuit are on, exciting transistors Q3 and Q4 are off.

In order to turn off one power transistor, its relating excitation transistor is to be turned on. Current flows via R46 through D14 to the winding of T2. The excitation voltage on the base of the power transistor and positive feedback cause the transistor to go quickly into saturation. When the impulse is finished both exciting transistors (Q3 and Q4) turn off. The positive feedback disappears and overshoot on the transformer winding quickly turns on the power transistor. This process is then repeated with the other transistor. Q1 and Q2 alternating connects one end of the primary winding of T2 to positive or negative voltage. The emitter of Q1 (collector of Q2) is connected to the third winding of the exciting transformer T2 and taken from this is a connection to the primary winding of the main transformer T3 and capacitor C7.

In order to keep the output constant connections from the +12 V and +5 V outputs are fed back through R25 and R26 to the TL494 control IC. These voltages are only used as reference voltages for the output voltage stabilisation. The outputs feature a common coil on all voltages and works like a transformer thus providing compensation for irregular loading of individual overvoltages.

The internal 5 V reference regulator (pin 4) of IC1 goes to the reference voltage through the voltage divider of R24 and R19 to the inverting input (pin 2) of its error amplifier. The output of the power supply is seen through the voltage divider R25, R26 and R20, R21 on the non inverting input (pin 1). The C1 and R18 feedback circuit provides stability of the regulator. Voltage from the error amplifier is compared to the ramp voltage across capacitor C11.

When the output voltage is decreased, the voltage on the error amplifier is also decreased. The exciting pulse to the power transistors Q1 and Q2 therefore causes them to remain off for longer, the width of the pulse before the output coil is greater and the output power is increased.

The +3.3 V output is also stabilised for reasons explained previously. The +3.3 V output is fed back to the shunt regulator TL431C. When the voltage on the +3.3 V output increases, transistor Q13 is turned off more and negative pulses across diode D32 decreases the output voltage.

The overvoltage protection circuitry composed of Q5 and Q6, monitors all of the output voltages and when some limit is exceeded the power supply is shut down. If a positive voltage appears at the base of Q6, it turns off thus turning off Q5and resulting in the +5 V from pin 14 of IC1 through D11 being seen on pin 4. This results in the power supply being blocked from operating as explained previously.

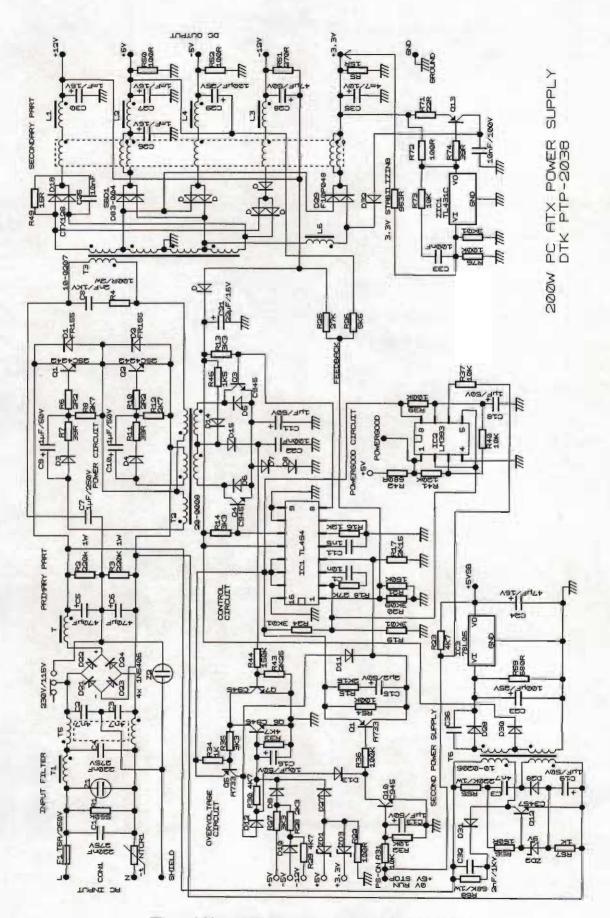


Figure 4-20 - 200 W PC ATX Power Supply Schematic

4.5 Television/VCR Power supplies

Television power supplies have not evolved much over the past decade and a half. There has not been standard power supply specification designs developed as seen previously with personal computer switch-mode power supplies. They are usually generic across the product ranges. Video cassette recorders utilise much the same switch-mode power supplies as televisions. Modern expensive plasma screen televisions have a new power supply arrangement which has proven to be highly sensitive to power system disturbances. According to Dr. Jovica Milanović [32] there has been many reports of damage to these televisions from supply disturbances.

They usually contain at least one switch-mode power supply – the main input power supply and a flyback derived non-isolated power supply in the horizontal deflection circuit.

The main input supply is used not only to generate the required d.c. output voltage levels for the internal circuitry but also to provide isolation through the high frequency transformer and feedback device (transistor or optoisolator) from the mains a.c.

Although it proved difficult to source television/VCR power supply schematic diagrams, some were gathered and appendix F contains example schematics obtained from the internet.

The Panasonic video cassette recorder schematic, obtained from Samuel M. Goldwasser's website on troubleshooting and repair of various electronic equipment [33], was used in a wide variety of VCR clones through the 80's and 90's and is still used today.

The circuit shown in Figure 4-21 is a typical switch-mode power supply found in television and video recorders. The actual supply is from a "Hi-Beam 250 Video/Data Projection System." This actual supply was electromagnetic compatibility tested as part of this research, which is discussed in Chapter 5. The d.c. output filter stage (which had to constructed for the experiment section) is shown in Figure 4-22.

The power supply incorporates protection circuitry and control circuitry to prevent the output changing and damaging internal components. It also includes an electromagnetic interference (EMI) filter on the input to reduce distortion of the mains supply.

This old design power supply is a self-oscillating operating power supply. The power switching transistor (BU326A) operates at a frequency of 30 kHz. The bridge rectifier, D5, converts the a.c. mains into 300 V d.c. which charges C13. R12 is a bleed resistor to discharge C13 when the power supply is turned off.

When the transistor TR2 is conducting, energy is stored in winding 1-15 of the transformer T1. When TR2 is not conducting, the stored energy in the magnetic field around T1 collapses. A voltage is induced in winding 4-6, 8, 10 which feeds five pulses to the d.c. supply panel (shown in Figure 4-22 to be rectified and smoothed before the output. The pulse amplitudes are dependent on their transformer tap-off points.

As the energy in winding 1-15 collapses, feedback by winding 13-11 causes the switching transistor TR2 to conduct again. Thus the power supply circuit is seen to behave as a self oscillating blocking oscillator.

Although the power supply is self-oscillating, it is not self-starting. On the positive half-cycle of the mains, diode D8 conducts and via the differentiating circuit (C15, R14 and R15), produces a positive going pulse to the base of TR2. These positive going pulses trigger and synchronise the 30 kHz oscillations.

Controlling the peak collector current and the duty cycle of TR2 the output can be regulated. When TR2 conducts, the d.c. voltage across the bridge rectifier flows in primary winding 1-15 and causes a linearly increasing current to flow in the primary. The voltage produced across the secondary winding is such that the rectifying diodes on the d.c. supply panel are all reversed biased.

Thyristor TH1 controls the duty cycle of the switching transistor. As the current increases, the positive voltage across R8 increases the gate potential of TH1 and the thyristor fires. When TH1 fires the positive plate of C7 reverse biases the base-emitter junction of TR2 and switches it off. During cut-off of TR2 the base goes negative, D6 conducts and charges the negative plate of C8 which will hold the gate of TH1 off.

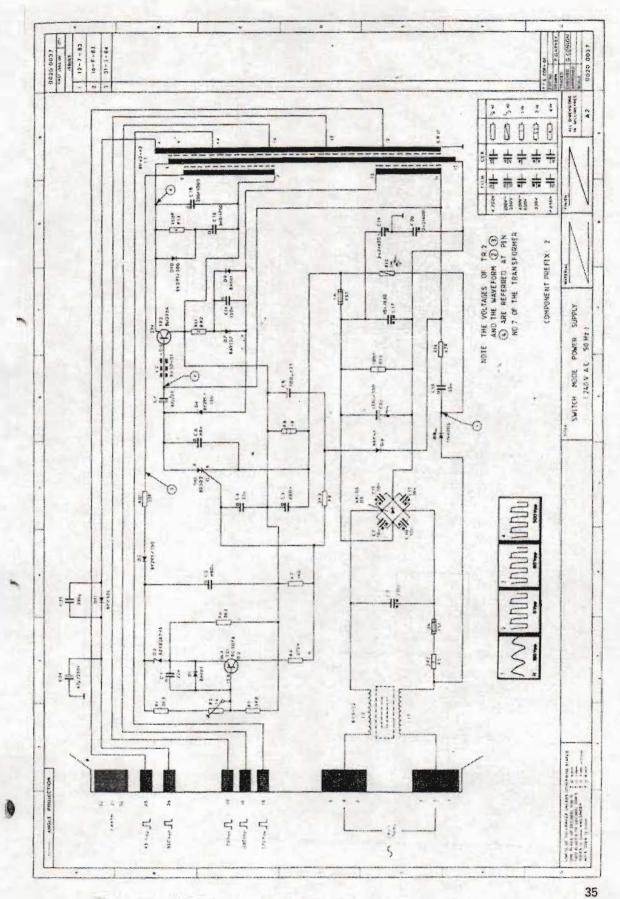


Figure 4-21 - Hi-Beam 250 Projector Switch-Mode Power Supply Schematic

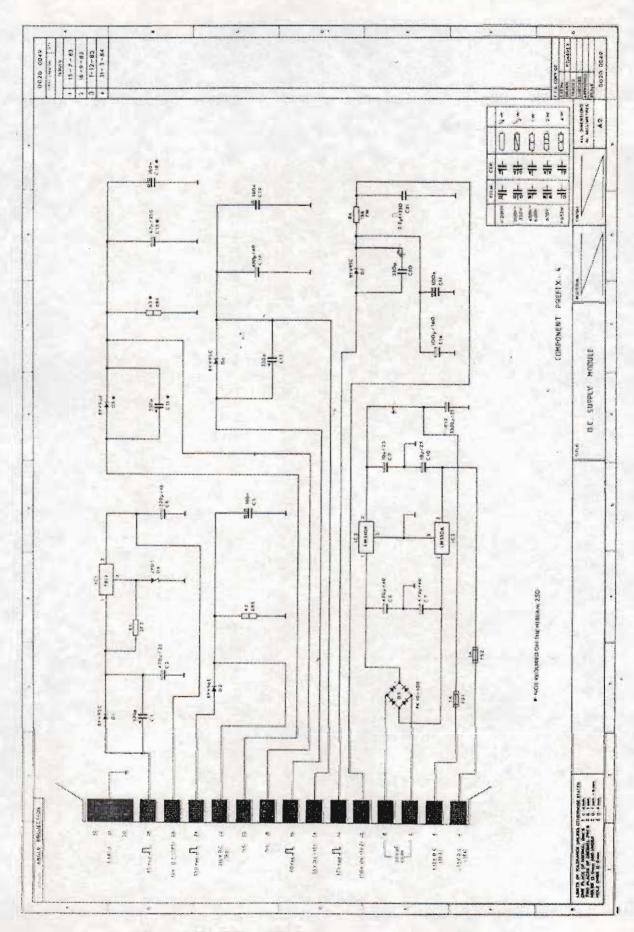


Figure 4-22 - Hi-Beam 250 Projector DC supply panel schematic

4.6 Conclusion

As can been seen the majority switch-mode power supplies use basically the same technology. They are considered the main, and probably the most understated, component of an appliance and can also act as a protection device for the appliance.

Their invention has solved many problems and enabled further advances in technology. Although due to their operation they have introduced additional problems. Due to the non-linear nature of the current drawn by the supplies they have made the issue of harmonics on the supply system a lot more prevalent.

The increased design complexity and component count has made them more susceptible to upset than their linear operation counterparts. However, the benefits of the switch-mode power supply significantly outweigh its disadvantages.

Chapter 5 Electromagnetic Compatibility Immunity Testing

5.1 Introduction

The intention here is to perform disturbance tests on domestic appliance switch-mode power supplies. An entire operational computer was also tested so to investigate the effect the disturbances have on the end user and on the work they may be doing at the time. The switch-mode power supplies themselves were to be subjected to various common disturbances, as outlined in Chapter 2. The test configurations and levels were determined from the European electromagnetic compatibility 61000 standard series (discussed in Chapter 2 and in the accompanying workbook). They outline the minimum disturbance limit strengths that these type of equipments should be manufactured to withstand. Using these values, the tests were carried out on either side of the limit level to assess if the power supplies were performing in accordance to the standards they are expected to meet.

Figure 5-1 shows a simple schematic depiction of the experiment. A full detailed schematic is shown in section 5.3. The disturbance generator is placed between the piece of equipment being tested and the mains input. It couples the disturbances onto the mains input conductors and outputs the disturbance and mains signal to the equipment being tested. The following sections describe the test generator and measurement equipment used in the experiment.

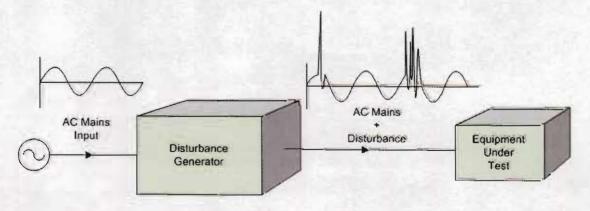


Figure 5-1 - Simple experiment schematic

Table 5-1 shows a brief summary of the tests that were performed on the power supplies etc. The following section describes in greater detail the equipment used, the equipment tested as well as the test procedures and results.

Tests Performed	Description	Standard
Harmonic Emission	Measurements of harmonic emission content	EN 61000-3-2
Power Quality Tests – Voltage Dips and Interruptions	Applying dips and interruptions on the input and assessing performance	EN 61000-4-11
Burst/ Fast Transient Immunity Tests	Applying rapid bursts to the input and assessing performance	EN 61000-4-4
Surge Immunity Tests	Adding voltage surges on the input and assessing performance	EN 61000-4-5

Table 5-1 - Testing Performed

5.1.1 Equipment Tested

Personal computers and television/video recorders were chosen as examples of domestic appliances that commonly experience voltage disturbance problems. The power supplies of these devices were sourced and tested. This is adequate since the power supply is the first point of entry within the appliance and thus is the first piece of circuitry the disturbance will strike. If the power supply cannot deal with the disturbance and it passes through into the more specialised operational circuitry inside, and damages it, then the appliance can become a lot more expensive to repair, most often needing to be replaced. The circuitry within the appliance is highly susceptible to voltage disturbances and anomalies due to sophisticated components used and the low voltage needed for operation. The purpose of the power supply is to take the 230 V 50 Hz a.c. input (120 V 60 Hz in the United States) and convert it to a much lower sustainable d.c. voltage level. Recent times have seen switch-mode power supplies become standard practice for this purpose. Their light weight and relatively inexpensive construction has seen them become part of nearly all domestic appliances, from personal computers to even fluorescent light bulbs. Their operation and purpose is much the same in most domestic

appliances thus testing a number of these switch-mode power supplies can be generalised to cover a wide range of appliances.

- To cover a number of years of personal computers (since not everyone can afford to upgrade computers every year) and also the time period indicated by the utility company in their correspondence as being a time of many failures and repairs, three LPX form factor PC switch-mode power supplies were tested.
- Also to cover more modern computers one ATX form factor PC switch-mode power supply, the LPX successor, and a microATX form factor power supply were tested. An equivalent form factor chassis and motherboard were needed to supply the power supplies with the power good signal to make them operational. A full list of the computer power supply specifications can be found in appendix D and details of these power supplies were covered in Chapter 4.
- A fully operational computer including monitor was also tested in order to see what affect the end user would experience as a result of such disturbances.
- A switch mode power supply, as previously described, from a projection unit –
 the d.c. supply panel of which had to be constructed was also tested. This unit
 is the same as those used in televisions and video recorders. The 150 V d.c.
 output of the switch mode power supply was loaded with a 100 W bulb.
- Two television/video recorder switch-mode power supplies were also tested.

5.2 Test and Measurement Equipment

The following section outlines the equipment tested in the investigation for electromagnetic conformity and also discusses the test equipment used during the tests.

5.2.1.1 Schaffner BEST 96 EMC Disturbance Generator

From researching disturbance generators that are available the *BEST 96 EMC* disturbance generator by *Schaffner* (see Figure 5-2) was chosen as the most suitable test instrument to hire.

The BEST 96 EMC is part of the Best family range of bench instruments which incorporates six EMC (electromagnetic compatibility) pulse test procedures in the one single housing. In the market it is aimed at manufacturing companies so they can test their products for compliance with the relevant standards. The instrument couples the disturbances onto the mains supply of the device unit being tested. The test parameters are user-adjustable above and below the limits set down in the standards.





Figure 5-2 - Schaffner Best 96 EMC disturbance test generator

The generator can perform four different EMC tests:

- Burst/Fast Transients
- Surge Immunity
- ESD (Electrostatic Discharge)
- PQT (Power Quality Tests) i.e. voltage dips and interruptions

Burst/Fast Transients

As mentioned previously fast transients are high frequency impulse spikes that occur on the mains, commonly caused by switching operations on the power lines. These high frequency spikes travel throughout the supply network and can therefore affect other equipment connected on the supply system. The most susceptible to damage from this phenomenon would be modern electronic devices (especially ones running at higher speeds). Data loss or malfunction of the device could result. The Best instrument injects a series of pulses into the equipment under test (EUT) at user set intervals and frequency as defined in the EN61000-4-4 standard [34]. The details of which will be discussed later in section 5.3.4.

The Best instrument allows the user to customise the following settings for a burst/fast transient immunity test:

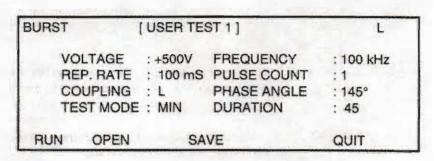


Figure 5-3 - Schaffner Best EMC Burst/Transient settings

Voltage: Burst output voltage Frequency: Frequency of the pulses within a burst Time from one Burst to the next Rep. Rate: Pulse Count: Number of pulses within a burst To which mains line the pulses are to be connected Coupling: Pulses coupled internally to Live N: Pulses coupled internally to Neutral PE: Pulses coupled internally to Earth L-N: Pulses coupled internally to Live and Neutral L-PE: Pulses coupled internally to Live and Earth L-N-PE: Pulses coupled internally to Live, Neutral and Earth Phase Angle: The angle in the EUT mains cycle at which the Burst will begin Test Mode: Test duration. Works in combination with the Duration setting SEC, MIN, HRS, Count, Continuous Duration: Specifies for how long a test will run

Surge Immunity

Surges are low frequency pulses containing considerable energy. Common causes of surge disturbances are a result of lightning strikes or heavy loads switching off on the utility supply network. The entry point of equipment would be the most susceptible to damage or upset. Input circuits and power supplies therefore are the most common found areas of failure as a result of surge disturbances. Nowadays even these power supplies are becoming more based on micro-electronics technology, resulting in greater vulnerability to surge induced damage.

The Best EMC instrument couples the surge waveforms as set out in the EN 61000-4-5 standard. The surge test waveforms were shown previously in Figure 2-9 and Figure 2-10.

There are two test generator characterising waveforms listed in the standard: the Combination Wave (or Hybrid) generator (1.2/50 $\mu s - 8/20 \mu s$), and the 10/700 μs generator. The latter, according to annex A of the standard, is only used to test class 5 ("Electrical environment for electronic equipment connected to telecommunication cables and overhead power lines in a non-densely populated area"). The area of interest here, fits classification class 3 ("Electrical environment where cables run in parallel") and therefore the combination wave (Hybrid) generator is only applicable to this experiment.

The Best instrument allows the user to adjust the following settings for the surge immunity tests:

SURGE		[USER T	EST 2]	L
7 7 7 7 7	LTAGE		OUTPUT F	Ri : 12 Ω
	PRATE			
CC	UPLING	: L-PE	PHASE AN	IGLE: 40°
TE	ST MODE	E: COUNT	DURATION	N : 100
RUN	OPEN	S	AVE	QUIT

Figure 5-4 - Schaffner Best EMC Surge settings

Voltage: Surge output voltage

Output Ri: Output resistance of the generator

Rep. Rate: Time from one Surge pulse to the next

Coupling: To which mains line the pulses are to be connected

L-N: Pulses coupled internally to Live and Neutral

L-PE: Pulses coupled internally to Live and Earth

N-PE: Pulses coupled internally to Neutral and Earth

L-N-PE: Pulses coupled internally to Live, Neutral and Earth

Phase Angle: The angle in the EUT mains cycle at which the Surge will begin

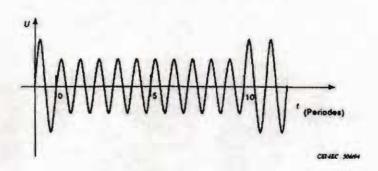
Test Mode: Test duration. Works in combination with the Duration setting

SEC, MIN, HRS, Count, Continuous

Duration: Specifies for how long a test will run

Voltage Dip and Interruption Tests

Voltage dips and interruptions (as discussed previously in sections 2.2) represent reductions in the nominal a.c. sinewave of varying value and duration, and are covered in the EN 61000-4-11 standard. Voltage variations (listed as optional in the standard) are not relevant here as they are not part of the experiment's criteria. The waveform as denoted in the standard is shown in Figure 5-5.



NOTE - The voltage decreases to 70 % for 10 periods. Step at zero crossing.

Voltage dips

Figure 5-5 - EN 61000-4-11 Voltage Dips Waveform

The Best EMC tests the devices under test by adjusting the output voltage to the EUT to levels set by the user on the instruments control panel. The settings that can be adjusted are as follows:

PQT	[USER TEST 1]	L
VOLTAGE	: 70%	
REP. RATE EVENT	: 60 S : 20 mS	PHASE ANGLE: 45°
TEST MODE	: MIN	DURATION: 5
RUN OPEN	SAVE	QUIT

Figure 5-6 - Schaffner Best EMC PQT settings

Voltage: The value to which the voltage drops, expressed as a percentage

Rep. Rate: Time from one event (i.e. voltage dip/interruption) to the next

Event: Duration in ms of dip/interruption

Phase Angle: The angle in the EUT mains cycle at which the event will begin

Test Mode: Test duration. Works in combination with the Duration setting

SEC, MIN, HRS, Count, Continuous

Duration: Specifies for how long a test will run

The BEST 96 EMC disturbance generator can also be interfaced and controlled via a PC connection and the appropriate software. The controls on the front panel were sufficient.

5.2.1.2 Tektronix THS 720P Digital Handheld Oscilloscopes

Tektronix THS 720P digital handheld oscilloscopes were used for these experiments. The Tektronix THS 700 series of oscilloscopes, to which the THS 720P scope belongs, combine real-time fully featured oscilloscope functionality and a true RMS digital multimeter. They are battery operated and their small design makes them easy for portable applications. The THS 720P oscilloscope is directed more towards electrical/power electronic applications. It adds harmonic analysis, power measurement and statistics and PWM motor drive triggering to the characteristics mentioned above.

Two of these THS 720P digital handheld oscilloscopes were required for the experiments.

In order to synchronise the scopes to capture the waveform the external trigger feature of the Best generator was used. The external trigger output was connected to the digital meter inputs of both scopes. When the generator performs a test disturbance it changes

the voltage on the external trigger signal simultaneously. Therefore by setting the scopes to monitor the external trigger signal they can be synchronised to capture the same disturbance waveforms.

Oscilloscope Probes

To select the correct probes for the application a number of factors were to be taken into account. The THS 720P scope has a bandwidth of 100 MHz. Therefore the voltage probes that were to be used with the scope should have at least the 100 MHz minimum bandwidth specification. The original probes that comes with the THS 720P scope is the P5102 high voltage passive probe. Its features are 100 MHz bandwidth, a maximum voltage rating of 1000 V_{RMS} and a 10X attenuation.

This scope was sufficient enough for the tests up to 1 kV. The transient and surge tests however required voltages above this value. The maximum voltage test limit required by the standards is 2 kV for the surge immunity test. However it was required to go slightly above this standard defined limit.

Knowing the rise time of the disturbance waveforms the bandwidth needed by the oscilloscope and probe can be calculated using the following formula:

$$Bandwidth = \frac{k}{rise \ time}$$

where **k** is a value between 0.35 and 0.45, depending on the shape of the oscilloscope's frequency response curve and pulse rise time response. Oscilloscopes with a bandwidth of < 1 GHz typically have a 0.35 value, while oscilloscopes with a bandwidth > 1 GHz usually have a value between 0.40 and 0.45 [35]. Therefore looking at the surge test, the rise time of the combination wave waveform is given as 1.2 μs. The bandwidth needed for this waveform is thus calculated to be approx. 292 kHz. For the burst/transient tests the rise time of one pulse is given as 5 ns. This corresponds to a 70 MHz bandwidth requirement. Hence the bandwidth of the scope is more than adequate.

After analysing the probes available and their suitability to the THS 720P scope on the Tektronix website, the *P5100 high voltage passive probe* was purchased. Its specifications feature a higher bandwidth of 250 MHz compared to the 100 MHz bandwidth of the scope. Since the scope's bandwidth is lower, then only this value can

be used, this is not a problem since at least it is not below the bandwidth of the scope. However its voltage rating of 2.5 kV is higher than the P5102 probe and meets the requirements of the experiment conditions. It also features 100X attenuation so this has to be set up accordingly on the scope when using this probe.

The Fluke 80i-110s AC/DC Current Clamp (shown below) was used for current measurements and harmonic analysis. It is compatible with the THS 720P scope.



Figure 5-7 - Fluke 80i-110s Current Probe

The current probe features are a selectable nominal current range of 10 A and 100 A a.c./d.c. with a corresponding continuous current range of 0.1 A - 1 A and 1 A - 100 A a.c./d.c. The output levels are 100 mV/A and 10 mV/A. It also has a zero error adjustment and is 9 V battery powered [36].

The THS 720P can be interfaced to a PC using the supplied RS 232 cable. Using special software available from Tektronix, called *Wavestar*, the data from the scope can be transferred onto the computer for analysis.

5.3 Experimental Setup and Procedures

5.3.1 Overview

As can be seen in Figure 5-8 the mains for both the Best 96 EMC disturbance test generator and the equipment being tested are fed off a typical 230 V mains supply in the laboratory. It should be noted that because of the earthing arrangement within the instrument, it should not be supplied from a circuit with RCD protection. An isolated protected earth connection was also needed for the ground plane and the test instrument.

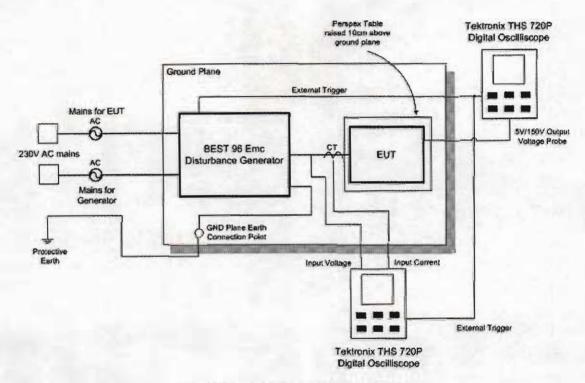


Figure 5-8 - Experiment setup schematic

The ground plane is necessary to ensure a good high frequency earth return path to the instrument is provided for. The earth block on the Best EMC generator is connected to the ground plane which in turn is connected to its own protective earth.

The perspex (non-conductive) plane, raised 10 cm, is to ensure there are no external voltage leakages and to exercise safety precautions. This test setup can be used for all the tests although the ground reference plane is only necessary for the fast transient burst tests but can also be used on the other tests.

The two THS 720P digital handheld oscilloscopes were needed for the experiments (as illustrated in Figure 5-8). On one scope input channel A was used to capture the input voltage disturbances into the EUT and the other input, channel B, used to monitor the current drawn by the supplies during the injected disturbances. The second oscilloscope was used to monitor the output on the devices under test - being the 5 V drive output on the computer power supplies and the 150 V output on the TV/projector switch mode power supplies.



Figure 5-9 - Experiment Setup Photograph

5.3.2 Harmonic Measurements

Before the main experiments using the disturbance generator were performed, the harmonic emission levels of the various power supplies where recorded. This was achieved using the Fluke 80i-110s current probe connecting into the THS 720P digital oscilloscope. The harmonic analysis feature of the scope was utilised. The collected data was uploaded to the computer for analysis via the Wavestar software.

As explained in appendix C, computer power supplies require a signal from the computers motherboard through the 'Power Good' line in order for it to start operating; therefore an appropriate motherboard is required along with the power supplies. (See appendix C for more on the operations of the PC power supply).

The harmonic measurements were recorded in the office, thus representing a typical everyday office environment. Firstly, the harmonic levels on the a.c. mains were measured. A linear load in the form of a 100 W 240 V bulb was used to load the mains in order to compare the current drawn by a linear load to that drawn by the non-linear power supplies. Figure 5-10 shows the voltage and current waveforms of the mains. It is seen that there is little current distortion present on the mains, although there does appear to be some "flat-topping" of the voltage waveform due to other non-linear loads that are affecting the supply system.

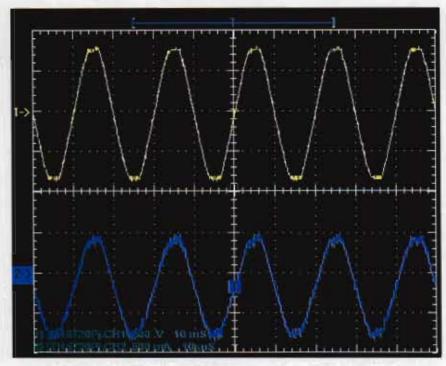


Figure 5-10 - Harmonics: Mains voltage and current waveforms

There is an overall current Total Harmonic Distortion (THD) of 4.886 % with the second and fifth harmonic showing only 3.633 % and 2.736 % of the fundamental respectively.

Figure 5-11 shows the harmonic content spectrum of the recordings.

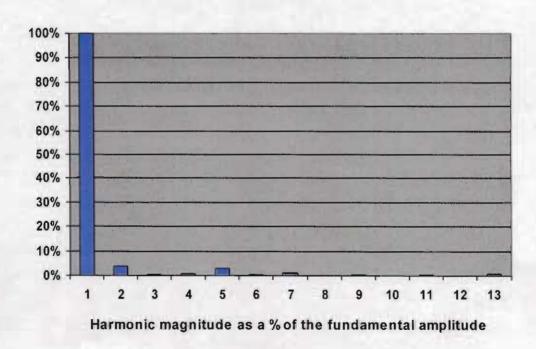


Figure 5-11 - Harmonic content of the mains supply

5.3.2.1 Harmonics Emission of the Projector SMPS

The full projector switch-mode power supply, shown in Figure 5-12, was loaded with a 100 W bulb on the 150 V d.c. output of the d.c. supply panel.

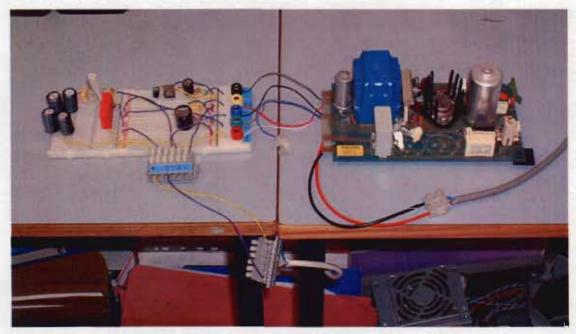


Figure 5-12 - Photo of the Projector SMPS and d.c. supply panel

Using the P5100 voltage probe and the 80i-110s current probe the following voltage and current waveforms were recorded.

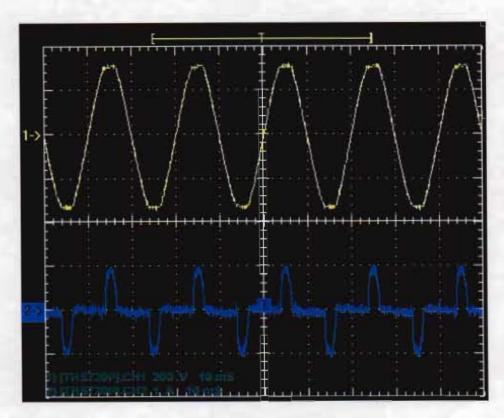


Figure 5-13 - Harmonics: Projector SMPS voltage and current waveforms

It is clear that the current waveform drawn is highly distorted. The current harmonic magnitudes expressed as a percentage of the fundamental magnitude are shown in Figure 5-14. The complete results obtained are shown in Table 5-2 and Table 5-3.

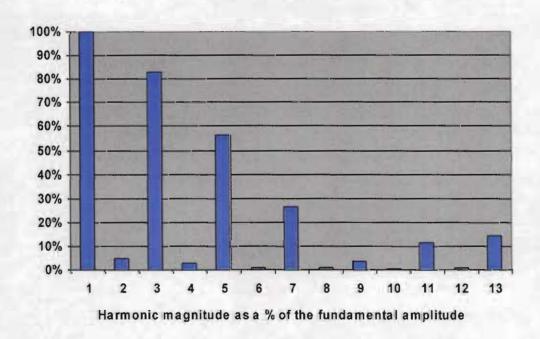


Figure 5-14 - Harmonic content of the projector SMPS

The full results obtained are as follows:

Voltage = 234.30 V	Current =	400.21 mA	True Power = 61.723 W	
Voltage THD = 3.083 %		Current Ti	THD = 105.704 %	
Power Factor = 0.658		Displacement PF = -5.2343		
Apparent Power = 93.770 VA		Reactive F	Power = 70.591 VAR	

Table 5-2 - Projector SMPS electrical characteristics

Harm No.	Freq. Hz	Voltage RMS	Voltage % of Fund.	Voltage Phase	Current RMS	Current % of Fund.	Current Phase
Fund.	50.025	233.88 V	100.0 %	0.0000	269.09mA	100.0 %	0.0000
2 nd	100.05	1.7425 V	0.745 %	160.79	13.514mA	5.022 %	178.12
3 rd	150.08	2.1343 V	0.913 %	92.520	223.61mA	83.099 %	5.3795
4 th	200.10	632.69mV	0.271 %	65.086	7.6760mA	2.853 %	49.235
5 th	250.13	5.9258 V	2.534 %	-6.3826	151.61mA	56.342 %	-166.58
6 th	300.15	556.16mV	0.238 %	82.072	2.0291mA	0.754 %	-126.69
7 th	350.18	2.4840 V	1.062 %	-177.80	71.265mA	26.484 %	16.600
8 th	400.20	286.58mV	0.123 %	163.45	1.9861mA	0.738 %	78.378
9 th	450.23	1.2497 V	0.534 %	6.7616	10.532mA	3.914 %	155.76
10 th	500.25	588.62mV	0.252 %	-98.317	853.95uA	0.317 %	-167.22
11 th	550.28	447.09mV	0.191 %	-94.783	31.409mA	11.672 %	-128.96
12 th	600.30	99.350mV	0.042 %	-65.529	2.0117mA	0.748 %	-45.942
13 th	650.33	417.74mV	0.179 %	84.343	38.548mA	14.325 %	48.792

Table 5-3 - Harmonic measurement results for projector SMPS

As can be seen above, the odd harmonics are prevalent and are the main reasons for the 105.704 % current THD. The third harmonic is high at 83.099 % of the fundamental.

This harmonic pattern is common to switch-mode power supplies. The charging profile of the input rectification capacitor on the d.c. link produces this result and is the main reason for the harmonic emission problems associated with the power supplies.

As discussed before, the standard relating to harmonic content is the electromagnetic compatibility standard EN 61000-3-2. The equipment under test here is classified under Class D specification. The limits set out in the standard for class D equipment are shown in Table 5-4 below. [37]

Limits for Class D equipment

Harmonic order	Maximum permissible harmonic current per watt mA/W	Maximum permissible harmonic current	
3	3,4	2,30	
5	1,9	1,14	
7	1,0	0,77	
9	0,5	0,40	
11	0,35	0,33	
$13 \le n \le 39$ (odd harmonics only)	3,85 n	See table 1	

Table 5-4 - EN 61000-3-2: Harmonic Limits for Class D Equipment [37]

The input power used to calculate the limits for Class D equipment, according to section 6.2.2 of the standard, is to be measured under the same test conditions as the harmonic current measurements. These were measured simultaneously.

Therefore applying the standard's limits to the results obtained the maximum permissible harmonic currents are obtained. From the true power value recorded of 61.723 Watts, the limits in mA's can be calculated.

For the 3^{rd} harmonic: 3.4 * 61.723 = 209.8582 mA

For the 5th harmonic: 1.9 * 61.723 = 117.2737 mA etc.

Table 5-5 compares the results obtained with the calculated standard permissible limits.

Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th
Standard Limit [mA]	209.86	117.27	61.72	30.86	21.60	18.28
Recorded Level [mA]	223.61	151.61	71.265	10.532	31.409	38.548

Table 5-5 - Odd Harmonics results and standard defined limits

As can be seen from the table, the recorded values highlighted with red text exceed the limits set out in the standard.

This piece of equipment, however, was manufactured before the standard limits were defined with the introduction of this standard in 2000 (the original introduced in 1995 and since been withdrawn).

5.3.2.2 Harmonic Emissions Results Summary

Similar harmonic measurements were made on the ATX, microATX and LPX form factor personal computer power supplies as well as on a complete Dell PC operating in normal mode and standby mode.

The results obtained from these power supplies were very similar and are summarised in Table 5-6.

Further details on these results can be found in appendix E.

Projector/TV Power Supply results									
Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th			
Standard Limit [mA]	209.86	117.27	61.72	30.86	21.60	18.28			
Recorded Level [mA]	223.61	151.61	71.265	10.532	31.409	38.548			

ATX/microATX PC Power Supply results									
Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th			
Standard Limit [mA]	103.020	57.57	30.30	15.150	10.605	8.973			
Recorded Level [mA]	110.24	80.332	48.014	18.659	4.8123	13.268			

LPX PC Power Supply results									
Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th			
Standard Limit [mA]	123.801	69.183	36.412	18.206	12.744	10.784			
Recorded Level [mA]	134.13	110.89	76.995	45.440	17.344	5.9423			

Fully operating Dell PC results									
Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th			
Standard Limit [mA]	195.599	109.31	57.529	28.7645	20.135	17.037			
Recorded Level [mA]	174.56	89.01	42.184	29.141	14.692	9.0974			

Fully operating Dell PC in standby results								
Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th		
Standard Limit [mA]	11.217	6.268	3.299	1.650	1.155	0.977		
Recorded Level [mA]	13.61	14.97	9.706	5.338	3.157	2.796		

Table 5-6 - Harmonic Emission Results Summary

5.3.2.3 Comments

The harmonic emission levels of the switch mode power supplies appear to exceed the limits denoted in the EN 61000-3-2 standard. This appears at least to be the case when they are lightly loaded. When the power supplies were fully loaded as in the Dell PC case the power consumption increased but the harmonic levels fell to a more acceptable level. However there is still high harmonic content being emitted by the supply. If in an office environment, where there could be many personal computer as well as fax machines and photocopiers etc. on the same supply, they could all accumulate on the supply system and may degrade the quality of supply being delivered to other equipment. As a point of interest, the Dell PC harmonic current emissions were also measured when the PC was set to standby mode (something many office computers are set at overnight). As can be seen from the table above the recorded harmonic emission content when is standby clearly exceeds the standards limits.

Neutral conductors in the modern office buildings have to be resized, to at least the same size as the phase conductors, because of the effects of these types of loads and the harmonic emissions that accumulate on it. Increased use of fluorescent lighting, which presents additional harmonics problems, are another reason as to why harmonics have to be considered in the building's wiring design.

5.3.3 Voltage Dips and Interruption Tests

These tests involve subjecting the EUTs to various voltage dips and voltage interruptions. They were performed first as they were expected to be the least severe and it was not expected that the power supplies would be irreparably damaged. The disturbance parameters are set of the European electromagnetic compatibility standard EN 61000-4-11: Voltage Dips, short interruptions and voltage variations immunity tests. The standard uses the rated voltage of the EUT as a basis for the voltage test level specification, here being 230 V.

A dip occurs when the nominal voltage drops by a significant percentage for a number of cycles. The standard specifies drops of 30 % and 60 % (i.e. the voltage drops from nominal value to 70 % or 40 % respectively). An interruption occurs when the mains voltage disappears altogether (for a value less than 5 % of the nominal voltage) for a number of cycles.

The P5102 voltage probe was used to capture the disturbance on the output of the Best EMC generator. The trigger setting on the THS 720P oscilloscope was set to receive the external trigger signal from the generator, as explained earlier. The acquisition mode of the scope was also set to single sequence capture to ensure the disturbance waveforms captured were held on the screen so they could be saved.

Another P5102 probe was also used to monitor the 5 V output of the PC switch-mode power supplies. This was to see if and how the disturbances affected the output of the power supply units. The 80i – 110s current probe was used to measure the current being drawn by the supply during the interference.

The tests were applied at 0°, 90° and 180° and for various time intervals.

Table 5-7 shows the full list of the tests performed, listing the settings inputted into the Best EMC generator (see section 5.2 for details on these settings):

	Voltage	Event	Phase Angle	Repetition Rate	Test Mode	Duration
Test 1	40 %	100 ms	0°	30s	Count	3
Test 2	40 %	100 ms	90°	30s	Count	3
Test 3	40 %	100 ms	180°	30s	Count	3
Test 4	70 %	10 ms	0°	30s	Count	3
Test 5	70 %	1000 ms	0°	30s	Count	3
Test 6	40 %	200 ms	0°	30s	Count	3
Test 7	40 %	500 ms	0°	30s	Count	3
Test 8	0 %	10 ms	0°	30s	Count	3
Test 9	0 %	10 ms	180°	30s	Count	3
Test 10	0 %	20 ms	0°	30s	Count	3

Table 5-7 - Power Quality Test Settings

Additional phase angles (45°, 90°, 135°, 180°, 225°, 270° and 315°) were tested for some of the supplies, however from these results it was not deemed necessary to repeat all of these for each EUT, so the table shown was used as it highlights the severities of the test range.

Waveforms were captured and saved for each of the tests but there are too many to reproduce here. The tests produced similar results for each power supply. The following are typical waveforms and results from some of the tests performed and these highlight the main observations to be made from these tests.

5.3.3.1 Test 1 on LPX form factor switch-mode power supply

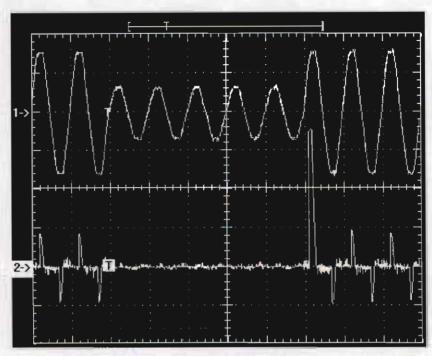


Figure 5-15 - PQT: Test 1 input voltage and current waveforms

Figure 5-15 shows the voltage being abruptly reduced to 40 % of the nominal value at a 0° phase angle for 100 ms (5 cycles). Looking at the current waveform, prior to the voltage dip the power supply was drawing current 'peaks' when the voltage reached a specific value (dictated by the choice of capacitor used at the d.c. link within the power supply). These current peaks depict the recharging of the capacitor. When the voltage was then reduced to 40 % the peaks disappeared. The input voltage was not reaching the level needed for the input capacitor to recharge and thus the charge within the capacitor was supplying the power supply with the voltage needed to continue operation. However as the capacitor charge is dissipating, the power supply could shut down if the voltage was not restored in time.

An inrush current peak of 3.53 A (this value is limited by the selection of capacitor used) is seen when the voltage is restored to its nominal 230 V value after the 5 cycles. The inrush current is due to the sudden increase in voltage which the capacitor uses to restore its charge as it had at that point a small amount of charge stored within it. Once the capacitor is 'recharged' the power supply returns to its normal operating conditions.

The 5 V d.c. output feeding the drives in the PC was not affected at any time during this voltage dip. The control circuitry within the power supply itself played its part in maintaining the constant output.

Another example to illustrate the effect the reduced voltage has on the input is shown in Figure 5-16. These waveforms, from *Test 4*, show the 70 % voltage reduction for just half a cycle caused the capacitor's charging peak to be cancelled with a slight increase in the next peak after the voltage was returned. This again was due to the capacitor depleting more of its charge than normal during the dip.

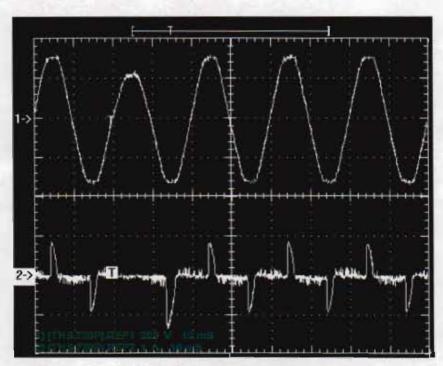


Figure 5-16 - PQT: Test 4 input voltage and current waveforms

5.3.3.2 Test 5 on LPX form factor switch-mode power supply

For this test the voltage was dropped to 70 % nominal for 1000 ms (1 second \equiv 50 cycles) at 0° phase angle. The waveforms in Figure 5-17 show the same phenomenon experienced during the previous tests where the capacitor tries to supply the power supply circuits with the current needed after the voltage was reduced. It no longer drew its charging 'peak' currents. The increased duration of the voltage dip in this test meant the capacitor had to recover its charge and the 70 % (\sim 161 V) reduction was not low enough to cause the power supply to shut down. After approximately 6 cycles the capacitor was able to adapt to the lower voltage and began recharging itself as before and settled into a new steady state pattern but this time drawing more current than when operating at the nominal voltage of 230 V.

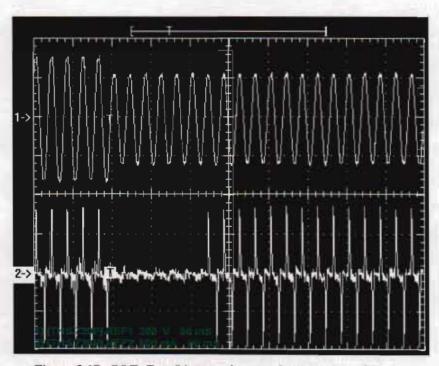
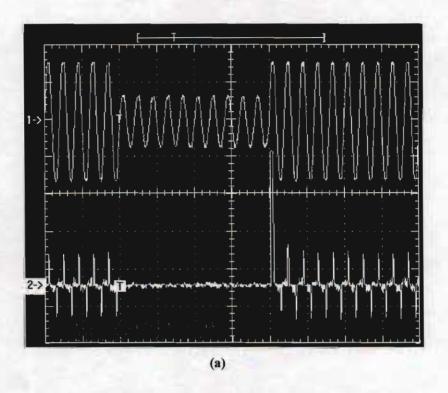


Figure 5-17 - PQT: Test 5 input voltage and current waveforms

When the voltage returned back to its nominal value (not shown in the figure) there was a small inrush current peak after which the current drawn returned to its normal operating state as seen on the left in the waveform. The 5 V output was not affected during this disturbance.

5.3.3.3 Test 6 on LPX form factor switch-mode power supply

The voltage for this test was reduced to 40 % (~ 92 V) for duration of 200 ms (10 cycles) at 0° phase angle. The waveforms are shown in Figure 5-18.



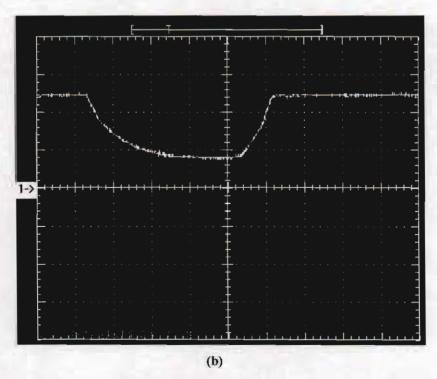


Figure 5-18 - PQT: Test 6 input voltage and current (a) and 5V output (b) waveforms

As the waveforms above indicate, the extended time period to 200 ms over Test 1 has affected the output of the power supply. This indicates that the charge within the input capacitor has depleted some time after the reduction in voltage and the 40 % voltage dip was too much for the power supply to adjust to in order to draw more current to sustain the output levels. Therefore the output of the power supply experienced a gradual drop to 1.51 V. The dip however only lasted 20.22 ms, and commenced approximately 179 ms after the voltage reduction suggesting at this point the charge within the capacitor had run out. When the voltage was restored the 5 V output took a further 4.44 ms to recover.

During these tests the CD-ROM tray was left open and extended. During this test the disturbance prompted the CD tray to retract in. This generally occurs, depending on the model of CD-ROM drive, when the supply has been lost to the PC and has caused the PC to suddenly switch off and reboot. Therefore it can be concluded, had this disturbance occurred whilst a user was working on the PC, the PC would have abruptly, without warning, switched off and restarted thus resulting in the user losing any unsaved data he/she was working on at the time. This of course is assuming that they did not have an Uninterruptible Power Supply (UPS) unit installed, which a very high majority of domestic users would not have.

Test 7 extends the above test to 500 ms, the output of which is shown in Figure 5-19.

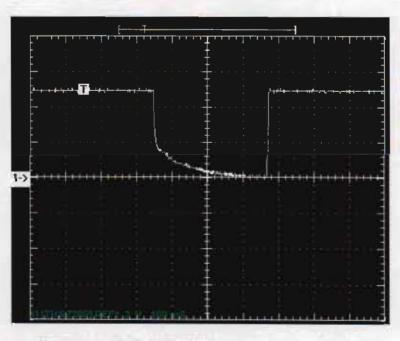


Figure 5-19 - PQT: Test 7 5V output voltage waveform

Here again the 40 % drop in the nominal voltage was not sufficient to enable the power supply to adjust and maintain a constant output. The entire dip itself lasted for approximately 321 ms thus indicating that after 179 ms (same as in test 6 before) the input capacitor's charge was used up. The longer duration in the dip this time enabled the output to completely fall to zero volts. When the voltage was again returned to 230 V nominal the output voltage also returned back to 5 V.

Again the CD-ROM tray retracted indicating that the PC again rebooted as a result of this disturbance thus causing the user to lose any unsaved data they would have been working on.

The results obtained on this LPX form factor switch-mode power supply in tests 6 and 7 can be classified under section 9 (b) on page 8 of the EN 61000-4-11 EMC standard. Section 9 classifies the test results of the equipment(s) under test on the basis of their operation during the test. Hence the results obtained in tests 6 and 7 under section 9 (b) are classified as "temporary degradation or loss of function or performance which is self-recoverable." [38]

The last three interruption tests had no affect on the output and the operation of the power supply since the durations at 10 ms and 20 ms were too short and the power supply was able to ride through the disturbances.

5.3.3.4 Performance of the other EUTs tested

The other two LPX form factor power supply units did not experience any such shutdown problems as illustrated above. This may be due to a higher value input capacitor being used. The input capacitors on these power supplies were 220 μ F (200 V) compared to 22 μ F (250 V) on the previous. These saw a peak inrush current during the tests of 5.1 A compared to the 3.53 A of the LPX power supply results described above. However, one supply did experience only a slight drop in the output voltage to 4.6 V during test 7.

When the fully functional PC (which had an LPX power supply installed) was tested the only test that yielded a result of interest was test 7. When the input voltage was reduced to 40 % for 500 ms the computer automatically switched off and restarted itself. The data entered prior to the test was indeed lost when the PC shutdown.

In order to find out how long the PC could withstand a 0 % interruption (since it passed tests 8, 9 and 10 without problem) the time was increased slightly to see at what point the PC consistently restarted. It was found that at 210 ms a complete abrupt reduction in the voltage caused the computer to reboot.

The ATX form factor power supplies however did not experience any problems when these tests were applied. In tests 6 and 7 the power supply managed to restore the current after just 5 cycles. However, the output of the power supplies during these tests did experience voltage dips to 3.6 V in both units but did not continue below the 3.6 volts.

The projector and TV switch-mode power supplies also did not experience any performance problems during these tests. They too exhibited, in tests 5, 6 and 7, the current restoring itself and drawing increased current after five to nine cycles.

5.3.4 Fast Transient / Burst Immunity Tests

The European electromagnetic compatibility standard EN 61000-4-4 outlines the range of test levels for testing equipment's immunity to fast transients/bursts. It also defines the test voltage waveform, set up and test procedure. The Schaffner Best EMC disturbance generator is designed to the standard's test specifications and to produce the defined waveforms.

In order to determine the correct test parameters, annex A of the standard needs to be consulted. Outlined here are five different levels of installation and environmental conditions that can be used to classify the piece of equipment being tested. The power supplies etc. tested here fit into the Level 2: Protected Environment description of annex A. [39]

The test limits, set on page 7 of the standard, for 'level 2' classified equipment is:

Open circuit output test voltage peak: 1 kV

Repetition rate of the impulses: 5 kHz

In the specifications for the generator on page 8 of the standard the burst period (i.e. repetition rate setting on the Best EMC generator) is to be 300 ms and the burst duration set at 15 ms. The pulse count setting can be calculated from the 15 ms burst duration and the pulse repetition rate within that burst as follows:

time =
$$\frac{1}{\text{freq}}$$
 \Rightarrow $T = \frac{1}{5 \text{ kHz}} = 0.2 \text{ ms}$

Pulse Count =
$$\frac{15 \text{ ms}}{0.2 \text{ ms}}$$
 = 75

The generator specs also say to apply the bursts asynchronously i.e. randomly on the mains waveform.

On page 11 it states that "the test voltage shall be applied between each of the power supply conductors and the protective earth at the power supply outlet to which the EUT is to be connected." From this statement the L-N-PE setting for the coupling method in the Best EMC generator was selected.

The duration of the test was also specified to be "not less than one minute."

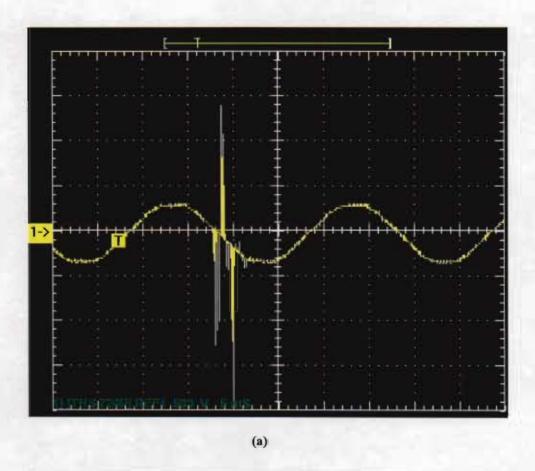
The tests performed are shown in Table 5-8 below:

	Voltage	Rep Rate	Freq.	Pulse Count	Coupling	Phase Angle	Test Mode	Duration
Test 1	+/- 800V	300ms	5 kHz	75	L-N-PE	Asynch	MIN	1
Test 2	+/- 900V	300ms	5 kHz	75	L-N-PE	Asynch	MIN	1
Test 3	+/- 1000V	300ms	5 kHz	75	L-N-PE	Asynch	MIN	1
Test 4	+/- 1050V	300ms	5 kHz	75	L-N-PE	Asynch	MIN	1
Test 5	+/- 1100V	300ms	5 kHz	75	L-N-PE	Asynch	MIN	1

Table 5-8 - Burst/Fast Transient Test Settings

The P5100 high-voltage probe was used on the output of the disturbance generator as well as the 80i-100s current probe. A P5102 voltage probe was used on the output of the EUT. Due to the quick repetition on the bursts the scope had to set from 'Single Acquisition' mode to 'Hold Button Only' (manually pressing the hold button on the oscilloscope to capture the waveform on the screen) in order to capture example waveforms of the transient bursts.

Figure 5-20 shows an 800 V burst coupled between live, neutral and earth and applied asynchronously to the input sine wave. The sample rate of the scope was set at 5 MS/s (corresponding to a time scale per division of 5 ms). The magnification setting of the scope was also used (shown in (b)) resulting in an increased sample rate to 500 MS/s. A peak of 1.4 kV and -2.12 kV minimum is observed.



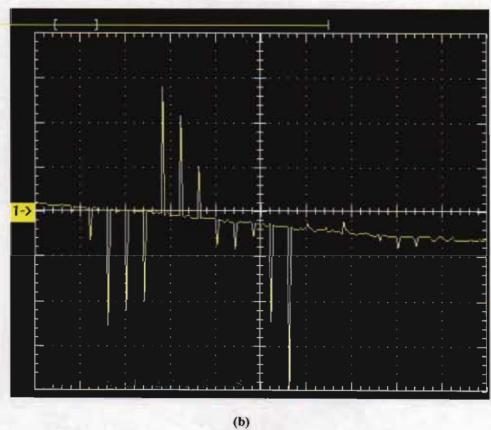


Figure 5-20 - Transient Burst Tests: 800 V input Burst L-N-PE

None of the computer power supplies, the projector/TV power supplies and the fully functioning computer experienced any problems as a result of these tests. They all performed normally during and after the tests, even when the burst voltage was increased above the limits set by the standard.

One thing to note though, when viewing the output of the supplies on the scope, the transients did appear to pass through the power supply and into the internal circuitry of the computer, television etc.

The level of transients on the output was indeed significantly higher than the 5 V output expected, (generally peaks reaching between 40 V and 80 V).

Figure 5-21 shows example waveform captures on the 5 V output of a computer power supply.

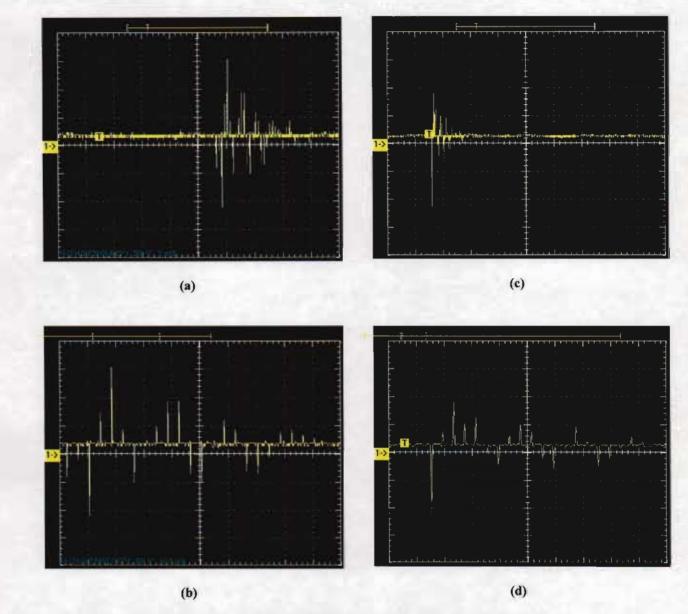


Figure 5-21 - Transient Burst Tests: 1 kV Bursts L-N-PE reflected on the 5 V output of a PC supply

(a) Ex. 1: 62 V_{max} and -44 V_{min}: 125 kS/s (b) Ex. 1 magnified: 12.5 MS/s

(c) Ex. 2: 36.8 V_{max} and -45.6 V_{min} : 50kS/s (d) Ex. 2 magnified : 5 MS/s

The burst test is a low energy test, and as such, it is not destructive. It is however stressful on digital equipment with high clock frequencies. Tests of this type have been reported to cause degradation of performance, loss of function, programmable failures, loss of memory stored and incorrect data processing [33] in equipment.

5.3.4.1 Further Testing

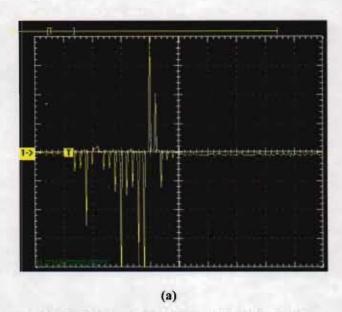
Considering the proposals being reviewed for inclusion in the EN 61000-4-4 standard in the coming years it was decided to re-test the specimens with the proposed changes to the transient burst waveform. It is under consideration to increase the repetition frequency specification of the generator in the standard to 100 kHz.

This is wise considering the constantly increasing clock frequencies of microprocessor applications. If a piece of equipment being tested were to have a clock frequency of 10 MHz, testing at 5 kHz tests only every 2,000th function state. The critical states are most likely to be within the 1,999 missed function states. If the testing was performed at 100 kHz or higher there is a greater chance of covering more states and, particularly in a development engineers case, this could help diagnose design problems.

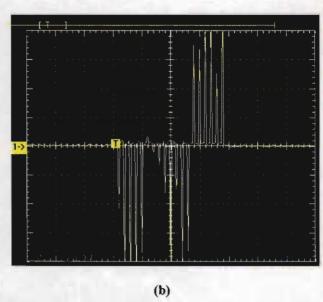
Switch-mode power supplies can operate at frequencies between 20 kHz and 100 kHz so testing them with the higher pulse repetition frequency should provide a more thorough test.

If the pulse repetition frequency is increased to 100 kHz, the burst duration will have to be brought down to 0.75 ms to ensure the same energy is injected into the equipment being tests. This corresponds to the same 'Pulse Count' setting of 75.

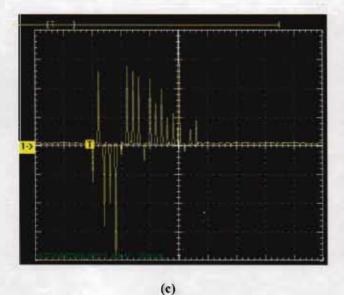
Waveform captures from these tests on an ATX form factor computer power supply are shown in Figure 5-22.



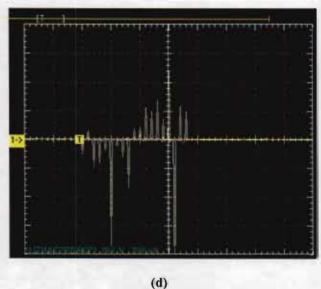
+ 1 kV Burst coupled L-N-PE with 100 kHz Pulses Scales: Y-axis: 5 kV X-axis: 200 μs 20.6 kV_{max} -25.6 kV_{min} (negative clipping)



+ 1.1 kV Burst coupled L-N-PE with 100 kHz Pulses Scales: Y-axis: 5 kV X-axis: 200 μs 25.6 kV_{max} (positive clipping) -25.6 kV_{min} (negative clipping)



+ 1 kV Burst with 100 kHz Pulses on 5 V output Scales: Y-axis: 50 V X-axis: 200 µs 200 V_{max} -256 V_{min} (negative clipping)



+ 1.1 kV Burst with 100 kHz Pulses on 5 V output Scales: Y-axis: 200 V X-axis: 200 μs 480 V_{max} -1.024 kV_{min} (negative clipping)

Figure 5-22 - Further 100 kHz pulse repetition transient burst test waveforms

As can be seen in the output waveforms above there is a significantly high transient voltage appearing on the output of the supply and entering the internal circuitry of the appliance – up to at least 1.024 kV.

As with the 5 kHz tests the devices tested were not damaged. This was the expected result due to the low energy content of the transient bursts that were applied. The full operating PC also did not experience any damage or upset and there was no disruption to the end user.

Although the electrical fast transients did not affect any of the devices tested, bursts for longer durations and/or higher intensity could damage or strain and degrade high sensitive (specialised) components within the appliance, as well as affect memory and data processing architecture. Especially if the transients were relatively frequent.

In addition if there are any components and/or software within the appliance that relies on the zero-crossing points in the waveform for timing purposes then transients can impact greatly. Since transients generally introduce a significant increase in zero-crossings during the disturbance, components reliant on this could produce errors and data corruption is highly probable.

5.3.5 Surge Immunity Tests

The final tests to be performed on the power supplies were the surge immunity tests as these were considered to be the most destructive of the tests.

The European standard governing surge immunity testing is the electromagnetic compatibility standard EN 61000-4-5: Testing and measurement techniques – Surge immunity test. This standard defines a surge as "a transient wave of electrical current, voltage, or power propagating along a line or a circuit and characterised by a rapid increase followed by a slower decrease."

In order to classify the equipment being tested annex A and B need to be consulted. These outline five different classes for equipment dictated by their environmental and installation conditions. The devices tested here fit under Class 3 in the annexes which is given the heading "electrical environment where power and signal cables run in parallel." The minimum surge limit class 3 equipment should be manufactured to withstand is 2.0 kV. [40]

Annex A of the standard also stipulates that for classes 1-4 the 'lightning' combination wave (hybrid) generator $(1.2/50 \mu s - 8/20 \mu s)$ is to be used for the tests.

The Schaffner Best EMC disturbance generator is designed to produce this combination wave as outlined and defined in the standard.

The positive and negative surge tests were coupled between Live and Earth and Line and Neutral. The output resistance (Ri) of the generator was set at 12 Ω which "represents the source impedance of the low-voltage power supply network and earth."

The tests were also performed at voltages on either side of the 2.0 kV limit and synchronised at 0° (the zero-crossing of the a.c. waveform), 90° (the positive peak of the a.c. waveform) and 270° (the negative peak of the a.c. waveform) so as to ensure the extreme cases where a surge could appear on the waveform.

Table 5-9 shows a full list of tests performed.

	Voltage	Rep. Rate	Output Ri	Coupling	Phase Angle	Test Mode	Duration
Test 1	+/- 1600V	30s	12Ω	L-PE/L-N	0°	Count	5
Test 2	+/- 1600V	30s	12Ω	L-PE / L-N	90°	Count	5
Test 3	+/- 1600V	30s	12Ω	L-PE / L-N	270°	Count	5
Test 4	+/- 1800V	30s	12Ω	L-PE/L-N	0°	Count	5
Test 5	+/- 1800V	30s	12Ω	L-PE/L-N	90°	Count	5
Test 6	+/- 1800V	30s	12Ω	L-PE/L-N	270°	Count	5
Test 7	+/- 2000V	30s	12Ω	L-PE/L-N	0°	Count	5
Test 8	+/- 2000V	30s	12Ω	L-PE/L-N	90°	Count	5
Test 9	+/- 2000V	30s	12Ω	L-PE/L-N	270°	Count	5
Test 10	+/- 2200V	30s	12Ω	L-PE/L-N	0°	Count	5
Test 11	+/- 2200V	30s	12Ω	L-PE/L-N	90°	Count	5
Test 12	+/- 2200V	30s	12Ω	L-PE/L-N	270°	Count	5

Table 5-9 - Surge Immunity Test Settings

Again the P5100 high-voltage probe was used on the output of the disturbance generator as well as the 80i-100s current probe. A P5102 voltage probe was used on the output of the EUT.

Figure 5-23 shows a waveform capture of a 1.6 kV surge applied between live and protective earth. A sample rate of 50 kS/s (the scope was also set to magnification mode effectively increasing the sample rate to 5 MS/s) was used to best obtain the surge waveform. The 1.5 kV maximum and a -340 V minimum was used to verify the waveform's shape in accordance with the waveform defined in the standard. It states that the negative dip in the waveform is to have no more than maximum 30 % of the peak. 30 % of 1.5 kV is 450 V and the dip in this waveform is within that so the wave shape in this regard is in accordance with the defined waveform.

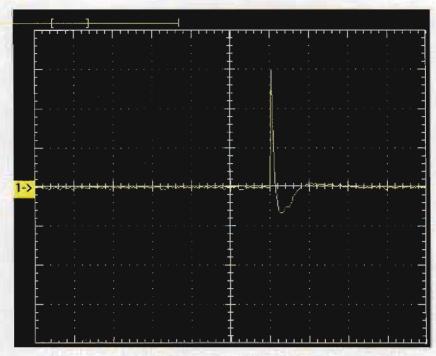
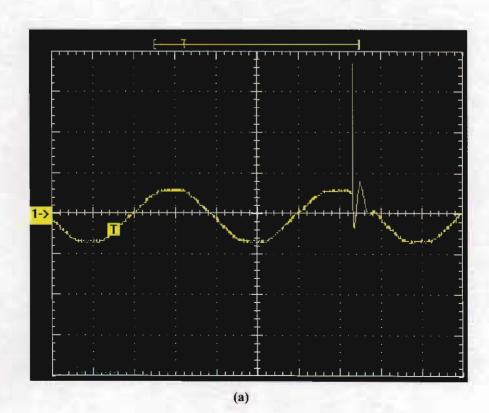


Figure 5-23 - Surge: 1.6 kV Surge L - PE @ 90° phase angle

A further example of an applied surge is shown in Figure 5-24. This figure shows a 2.0 kV surge applied between the live conductor and neutral at the positive peak of the waveform. Nothing significant was measured on the low voltage outputs when the surges were applied.



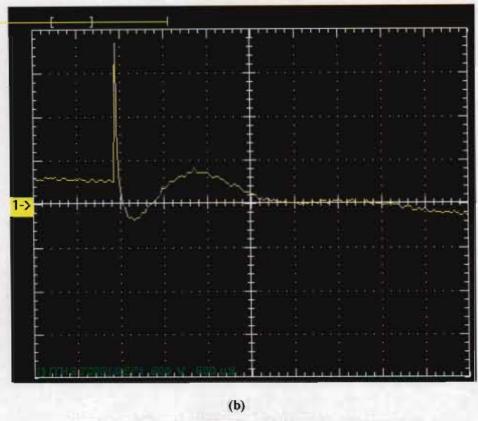


Figure 5-24 - Surge: 2.0 kV Surge L - N @ 90 ° phase angle

(a) ac mains signal & the surge applied at the positive peak (b) magnified image of the surge

Again these surge tests had little impact on the power supplies. None of them experienced any permanent damage and all continued operating normally after and during the tests. The output of the power supplies weren't affected greatly by the surges concluding that the overvoltage protection and also the feedback control in the power supply were responding fast enough.

However, on one computer power supply unit when a 1.8 kV surge was applied for the second time at a phase angle of 90° a loud bang along with a bright spark was observed within the power supply casing. The unit though, did not malfunction and continued operating normally as before. The test was applied again, and again the bang and spark was observed. The power supply was then taking apart to investigate the source of this 'bang and spark'. No components appeared to be damaged and no capacitors, as initially suspected, had "popped." The only sign was a slight scorch mark on the PCB board across the DC link after the input capacitors of the power supply circuitry. The reason for the flash and bang appeared to be just a design flaw where the two soldered nodes were placed too close together. The power supply was reconstructed and re-tested.

Again the same result was presented and was repeated as the rest of the tests were performed. The power supply did not fail from any of the tests though.

Although this phenomenon was not damaging to the power supply and did not affect the operation of the appliance it, however, is not desirable to have happened. It is a potential safety hazard and is dangerous for a normal domestic user. Since it occurred within the limits set by the standard it would have not passed the tests and would be described in the test results category (b) on page 14 of the standard which states it as "temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention." From this result the power supply could not be awarded the CE marking of conformity to the EMC standards and operational safety.

None of the other computer power supplies and fully functioning computer experienced this phenomenon, thus it appears to have been a one-off case.

The projector and TV power supplies also did not experience this phenomenon. The output of these supplies did experience a bit more variation than the computer power supplies but did not present consistent fluctuation. Hence, it is nothing to be concerned about.

5.4 Discussion

Harmonic emissions of the test subjects were first recorded. These were carried out as an exercise in harmonics to see how these power supplies, which are known to cause problems with third harmonic currents being fed back into the supply system, contribute to the harmonics problem and how they function in relation to the EN 61000-3-2 harmonic emissions limits standard. The power supplies when unloaded all exhibited harmonic emission content significantly above the limits set out in the standard. When a fully loaded and functioning personal computer was tested the harmonic current levels reduced and were within the limits. There was however high third harmonic content which is due to the nature of the operation of the input a.c. to d.c. rectification stage. If a number of these types of loads were to be connected on supply system in a relatively small area the harmonic emission currents could potentially add up and result in distorted voltage available to other appliances powered from the same electrical supply. Degradation and loss of performance would generally occur over time were the distorted 'dirty' supply could stress and weaken appliance components.

The voltage dip and interruption tests yielded some interesting results. The interest was not particularly in the area of damage to the power supply unit but more towards the end user's experience. The television and projector power supply units tested did not experience any problems (most probably due to a more robust design – they were heavier and used larger (and fewer) electronic components) while some of the computer switch-mode power supplies experienced problems with the test. Some LPX form factor power supplies, commonly used in PC's in the late 1990's, experienced computer restarts when applied with the 40 % voltage dips for longer lengths of time. The end user whilst working on their computer at the time would have lost any work they were working on. This of course is by no means acceptable.

The fully operating PC also experienced this same effect and consequences.

The modern ATX form factor power supplies did not experience this however, and they were able to ride through the dips and interruptions and adjust accordingly to ensure operation continued and the output voltages were maintained. Longer time lengths and increased voltage dips would of course eventually cause the power supply to shutdown.

But when tested with the limits set by the standards (limits they are meant to be manufactured to withstand), they passed without problem.

The fast transient/burst tests did not show up any problems with the power supplies. None of the units tested behaved abnormally and did not experience any problems or malfunction during these tests. From observing the scopes when the burst were being inputted into the EUTs, the effects of the burst disturbances were seen on the output of the power supply. This means that the burst transients were not 'dealt with' by the power supply, mostly probably because of the high speed and frequency of the transients. The transients therefore travelled through the power supply into the circuitry of the appliance itself. This could have destructive and damaging consequences to any highly sensitive components in the appliance. The circuits and the components within computers e.g. motherboards, graphics cards, modems, hard disks, RAM memory, microprocessors are far more sensitive and far more technologically advanced than the components in the power supply casing. They are highly susceptible to upset from voltage disturbances and variations. And as the technology of these components, especially microprocessors, continue to improve and become more and more microscopic, the need for perfect sustained voltage levels will also become highly prevalent and they will become less tolerant to anomalies in their voltage supply.

In time and/or if frequent, these fast transients will damage the internal circuitry of the appliances and thus incur a much higher repair bill and possible replacement of the whole appliance. Since just simple switching on the utility network can cause these transients to propagate on the mains supply considering transient protection devices such as TVSS's (Transient Voltage Surge Suppressor) and surge protection strips is advisable.

The most severe of the tests, the surge immunity tests, were performed last. These tests too did not result in much damage. The only incidents to affect the units tested was on one computer power supply where, surges from 1.8 kV resulted in a flashover on the d.c. link capacitor after the bridge rectifier as part of the input stage of the supply. This is within the 2 kV limit set by the EN 61000-4-5 surge immunity standard and is obviously not desirable to have happen within a domestic setting. The power supply continued working correctly after the flashover and was not damaged. No effect was seen on the output of the power supply so the operation of the computer would have

been maintained and the computer components would not have been damaged – at this level of surge.

The surges during the tests were not seen on the output of any of the units being tested thus indicating that the feedback control and overvoltage protection incorporated into the circuitry of the power supply units prevented the surge from passing through onto its output.

Arising from the email discussion from within the utility company it appeared that computers and televisions/VCRs were the main appliances that people were complaining about being damaged therefore it was decided to focus on these appliances. Since the power supply is the first point of entry into the appliances they were picked as the main subjects of focus.

Overall the units tested were not damaged. It can be concluded that today's modern switch-mode power supplies for these appliances are being manufactured to withstand the voltage disturbances they are supposed to withstand as set down in the EN 61000 electromagnetic capability series standards. However an LPX form factor computer switch-mode power supplies of just a few years ago and a fully operational PC from the same time with a LPX power supply installed failed to operate adequately during the voltage dip tests. They were not damaged though, as they only affected the data the end user was working on at the time.

One additional point of interest is the transient bursts that passed through supplies into the workings of the appliance. This could eventually lead to problems with the appliance if protection is not sought and/or the transients experienced on the electricity supply (if frequent) are resolved.

If an appliance is damaged then it is more likely that a disturbance of higher severity and/or longer duration than the limits set in the standards has damaged it.

The results obtained from these tests are consistent with the finding of L.M. Anderson and K.B. Bowes [2] as well as S.B. Smith and R.B. Standler [1]. They tested various consumer electronic equipment and found that transients do not produce any adverse effects on the equipment whilst voltage dips did result in loss of data and memory. [1] found that televisions and PC power supplies were the most vulnerable to upset and

damage from surges but the levels however that affected them were between 4 kV and 6 kV, higher than the permissible surge setting of the Best disturbance generator used here and higher than the limits set in the standards. The results obtained in the tests here corroborate the findings in this paper.

Chapter 6 Switch-mode Power Supply Simulations

6.1 Introduction

Having examined the various packages in Chapter 3, PSpice was chosen to be the best choice for the simulation of the switch-mode power supplies.

The student version of PSpice, from Cadence Design Systems Inc. [41], was used for the simulations. This version is limited to circuits with 64 nodes, 10 transistors, 10 transmission lines and 65 digital primitive devices. This is more than enough for the simulations required.

The approach taken was to start with basic d.c.-to-d.c. converter circuit simulations (as covered in section 4.3) and extended these to include the a.c. input rectification stage and then to implement feedback control on the circuit. Once the circuit behaves correctly the power quality disturbance tests of Chapter 5 were applied to examine the behaviour of the circuit in the presence of these disturbances.

PSpice Schematics and the PSpice Capture programs were initially used to construct the circuits. This method had the advantage of creating a visual schematic diagram of the circuits and when simulated the PSpice A/D program is called to display graphical simulation results.

The final method involved the use of circuit description text files (*.cir files) as it was easier to create the models for non-standard elements this way then in schematics. As explained earlier these files contain nodal descriptions of a circuit and when simulated in PSpice A/D graphical results can be displayed at any of the nodes.

6.2 Switch-mode power supply circuit

The d.c.-d.c. converter topologies were constructed in PSpice (shown in appendix G). They were extended to include a.c.-d.c. rectification on the input.

A complete switch-mode power supply circuit incorporating feedback control was built and tested and is shown in Figure 6-1.

As explained in section 4.3.7, a reference signal is taken from the output and this is fed into a comparator circuit that compares the output voltage with a reference voltage of the desired value. The error signal on its output is inputted to a pulse width modulator which accordingly controls the duty cycle of the switch in the circuit. By varying the duty cycle of the switch device the output voltage can be altered and therefore maintained constant.

With the aid of D.W. Hart's [28] book a PSpice .cir circuit description file was used to create the switch-mode power supply circuit in Figure 6-1.

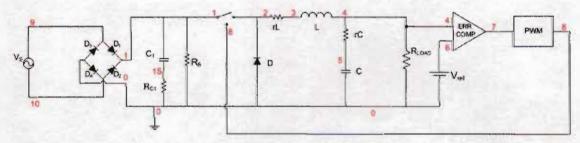


Figure 6-1 - Switch-Mode Power Supply Circuit Schematic

The complete .cir file for this circuit is as follows:

AC-DC Switch-Mode Power Supply Circuit

D1 9 1 DMOD

******** CIRCUIT AND CONTROL PARAMETERS ******* .PARAM Vm = 230 F = 50.PARAM CFILTER = 150uF .PARAM ICC = $\{0.9*Vm\}$.PARAM Vref = 12 .PARAM L = 100UH rL = 2.PARAM C = 80UF rC = .6.PARAM RLOAD = 5 .PARAM Vp = 3; (peak of ramp in modulator) .PARAM R1 = 1K C1 = 1.45 nFR2 = 33KC2 = 161pF ;error amplifier parameters VS 9 10 SIN (0 {Vm} {F})

```
D2 10 1 DMOD
D3 0 9 DMOD
D4 0 10 DMOD
C1 1 1S {CFILTER} IC={ICC}
RC1 1S 0 0.5
R8 1 0 180000
XSWITCH 1 0 2 8 SWITCH
rL 2 3 {rL}
L 3 4 {L}
          IC={Vref/RLOAD}
rc 4 5 {rc}
C 5 0 {C} IC={Vref}
R 4 0 {RLOAD}
                    ; compensated error amplifier
XCOMP 4 6 7 COMP
Vref 6 0 {Vref}
XMOD 7 8 MODULATOR ; PWM controller
********* R-C SNUBBERS TO HELP WITH PSPICE CONVERGENCE ****
.SUBCKT SNUB 1 2
RSNUB 1 3 10000
CSNUB 3 2 .1NF
. ENDS
XSNUB1 9 1 SNUB
XSNUB2 10 1 SNUB
XSNUB3 0 9 SNUB
XSNUB4 0 10 SNUB
****** COMPENSATED ERROR AMPLIFIER SUBCIRCUIT ******
.SUBCKT COMP 1 5 3
*TYPE 2 COMPENSATING NETWORK 1=INPUT; 5=+ (NONINVERTING INPUT);
3=OUTPUT
R1 1 2 {R1}
R2 4 3 {R2}
C1 2 4 {C1}
C2 2 3 {C2}
RIN 2 5 1E6
EAMP 3 0 TABLE \{V(5,2)\} (-15U,-15) (15U,15) ; saturation at +/- 15
volts
.ENDS COMP
******** PWM CONTROLLER SUBCIRCUIT ********
.SUBCKT MODULATOR 1 2
*pulse-width modulator -- converts amplified error to duty ratio
RX 1 0 1G
EMOD 2 0 TABLE {V(1)/Vp} (0,0) (1,1)
RY 2 0 1G
.ENDS MODULATOR
****** AVERAGED SWITCH MODEL SUBCIRCUIT INCORPORATING THE DIODE
* VORPERIAN'S SWITCH MODEL
.SUBCKT SWITCH A P C D
GAP A X VALUE {V(D)*I(VC)}
ECP X P VALUE=\{V(D)*V(A,0)\}
VC X C 0
RCONV D 0 1G
. ENDS SWITCH
. PROBE
.TRAN 10u 100m UIC
.MODEL DMOD D; Default diode
.END
```

The first section of the file contains the circuit parameters which are called in the circuit description. For instance, Vm is the voltage level of the a.c. source and is at a frequency of f = 50 Hz. Other circuit parameters are presented. A constant 12 V d.c. output is required from the 230 V a.c. input (mimicking a computer power supply). Therefore V_{ref} is set to 12 V and the rest of the circuit parameters are chosen to provide the sufficient smoothing on the d.c. outputs.

The equivalent series resistance (ESR) of the capacitor, C1, across the input rectifier is included and is taken from typical values given in a Radionics catalogue. The resistor R₈ is used as a bleed resistor for the capacitor. The input rectifier stage values are taken from the schematic for the projector SMPS described in section 4.5.

R-C snubbers were placed across the diodes in the bridge rectifier to correct convergence problems when the circuit was simulated, thus avoiding sharp discontinuities that resulted in PSpice proceeding with a very small time step when the simulation was run.

Sub-circuits for the switch, compensation error amplifier and the pulse width modulator are also described and called using the 'Xname' command in the circuit description.

The compensation error amplifier circuit, as covered by D.W. Hart [28] is shown opposite.

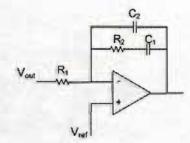


Figure 6-2 - Compensation Error Amplifier

The .TRAN statement calls for a transient analysis of the circuit and stipulates a printstep of 10 µs and the simulation to run for 100 ms.

Once the circuit of Figure 6-1 was performing correctly it was then subjected to the EMC tests described in Chapter 5. The simulation of these disturbances is described next.

6.3 EMC Disturbance Simulations

6.3.1 Voltage Dips Simulations

In order to simulate voltage dips on the circuit some modifications need to be made at the input of the circuit. To mimic voltage dips for a certain period of time the configuration shown in Figure 6-3 at the a.c. input proved to be only way to achieve this.

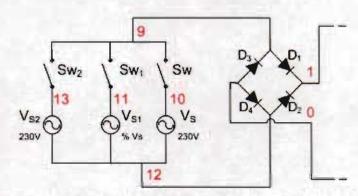


Figure 6-3 - PSpice circuit configuration for Voltage Dip on the Input

At time 0, switch Sw is closed and V_S operates on the input for a desired period before the voltage dip. When the voltage dip is required Sw opens and Sw_I closes simultaneously and V_{SI} operates. The voltage level of V_{SI} is set according to the level of dip the test requires. When the duration of the dip reaches a certain predefined value Sw_I opens and V_{S2} (which is set to the same value as V_S) takes over as Sw_2 closes.

The partial circuit file description for a voltage dip input of 40 % of V_S lasting for 100 ms is shown below:

The resulting PSpice waveforms are shown in Figure 6-4 and Figure 6-5.

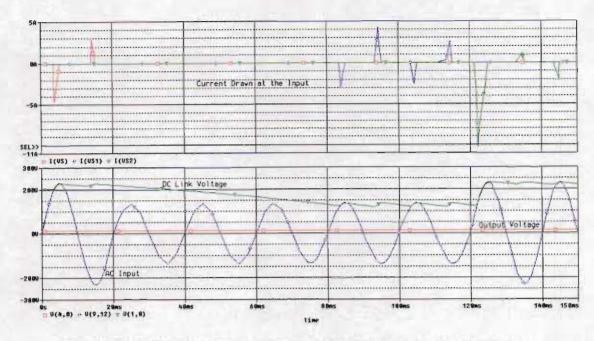


Figure 6-4 - 100 ms 40 % Voltage Dip Simulation - Current drawn and Voltages

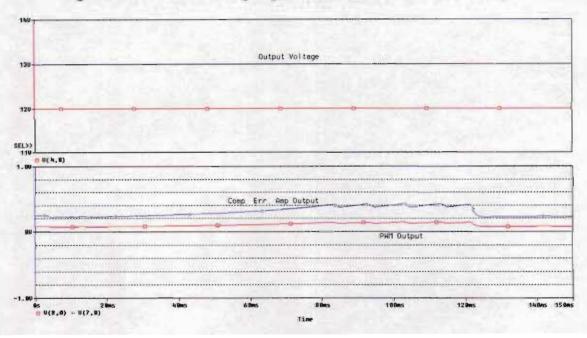


Figure 6-5 - 100 ms 40 % Voltage Dip Simulation - Output Voltage, Comp. and PWM Output

As the waveforms show, when the voltage dip occurs the current drawn ceases and the input rectifier capacitor C_I provides energy to the switching converter circuit. During the voltage dip the capacitor's charge continues to deplete until the voltage across it reaches the voltage dip level. Current then begins to be drawn again but the current pulse are higher than when at full voltage (ignore first current peak, as the circuit is not at steady state, and compare to the second red peak). Both the compensation error

amplifier and the PWM outputs gradually increase thus altering the duty cycle of the switch to maintain the constant 12 V output. When the voltage is restored these outputs return to normal state and there is an approximate 7.8 A current spike drawn to quickly recharge the capacitor.

This result would present a significant problem to the power supply components if voltage dips were a regular occurrence. The increased energy drawn will stress components their current level ratings may be exceeded. The increased stress would induce thermal ageing and cause increased heating in the bridge diodes. It could significantly reduce the power supplies life time and make it even more susceptible to failure from more severe disturbances.

The full range of voltage dip tests as shown in the Table 5-7 in section 5.3.3 were simulated with this circuit. Additional test circuit files and simulation results are contained in appendix G.

Table 6-1 gives an outline of a few of the tests simulated and the effects that would be expected in practice.

Test Parameters	Effect	Consequences Thermal ageing and component stress, reducing the life of the supply	
70 % dip for 1000 ms	Current peaks drawn during the dip ~ 1.5 times nominal value		
40 % dip for 500 ms	Increased current drawn during the dip	As above	
0 % dip for 120 ms	Loss of output after 105 ms	Appliance shut down	

Table 6-1 - Example voltage dip simulation results and effects

Voltage dips to levels above the output voltage (12 V here) for any duration does not cause the power supply output to change. The input capacitor (C_{filter}) however draws increased current to maintain the constant output. The choice of capacitor used dictates the point during the dip at which the power supply begins to draw current again. When a dip to at the output voltage level occurs there is not enough energy in the capacitor to maintain the output voltage.

Table 6-2 indicated typical effects voltage dips will have on the current peaks drawn by the power supply using a 150 μ F filter capacitor.

% Voltage Dip	Peak	Duration
0 %	2.8 A	1.1ms
40 %	3.9 A	3.3 ms
70 %	4.41 A	4.6 ms
85 %	4.5	8 ms *Output affected

Table 6-2 - Input Current at various voltage dips

6.3.2 Fast Transient Bursts Simulations

For these tests the input source configuration seen in Figure 6-6 was implemented.

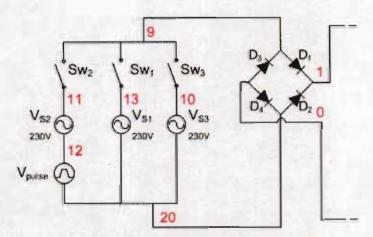


Figure 6-6 - PSpice circuit configuration for Transient Bursts on the Input

 V_{pulse} is used in conjunction with V_{S2} when impulses are required on the input. From time zero V_{S3} acts as Sw3 is closed. After, say, 5 ms the impulses are to be added to the input. Using the specifications in the EN 61000-4-4 EMC standard the burst is to last for 15 ms and contain impulses at a repetition rate of 5 kHz. As calculated in section 5.3.4 this equates to 75 impulses per burst. The bursts are to be repeated every 300 ms. A rise time of 5 ns and fall time of 100 ns for each impulse is used and the pulse description file is as follows:

VPULSE 12 20 PULSE(0 {3.478*Vm} 5M 5N 100N 1N 0.2M)

The 0.2 ms pulse period command is used to achieve the 5 kHz repetition frequency of the impulses. The peak voltage is implemented as a factor of V_m , in this case being 800 V impulses.

When V_{pulse} is used in series with V_{S2} set at the nominal 230 Vrms a.c., the result is the appearance of adding the bursts onto the input.

When the 15 ms burst duration is finished Sw2 opens and Sw1 closes resulting in the continuation of the a.c. signal, and when the burst period of 300 ms elapses V_{S2} and V_{pulse} conduct and the process is repeated.

The partial circuit file description for a 1 kV burst test follows.

```
*********** CIRCUIT DESCRIPTION ************
SW1 9 10 SCONT1 20 SMOD1
.MODEL SMOD1 VSWITCH (RON=.001)
VPULSE1 SCONT1 20 PULSE(0 5 20M 1N 1N 284.99M 300M)
VS1 10 20 SIN (0 {Vm} {F})
****************** V3 Source 0-5ms ****************
SW3 9 13 SCONT3 20 SMOD3
.MODEL SMOD3 VSWITCH (RON=.001)
VPULSE3 SCONT3 20 PULSE (0 5 0 1N 1N 4.99M)
VS3 13 20 SIN (0 {Vm} {F})
************* V2 source + burst repeated every 300ms on for
15ms **********
SW2 9 11 SCONT2 20 SMOD2
.MODEL SMOD2 VSWITCH (RON=.001)
VPULSE2 SCONT2 20 PULSE(0 5 5M 1N 1N 14.99M 300M)
VS2 11 12 SIN (0 {Vm} {F})
VPULSE 12 20 PULSE(0 {4.348*Vm} 5M 5N 100N 1N 0.2M)
```

Simulation waveform results are shown in Figure 6-7 and Figure 6-8.

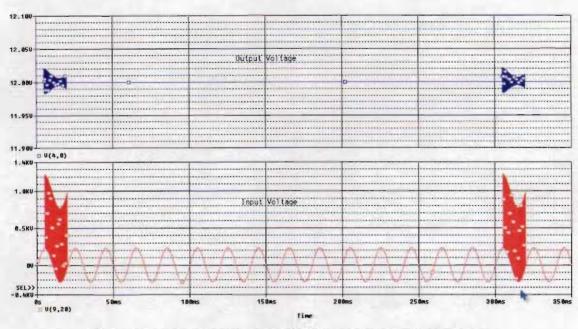


Figure 6-7 - PSpice 1 kV Burst Simulation - Input and Ouput Voltages

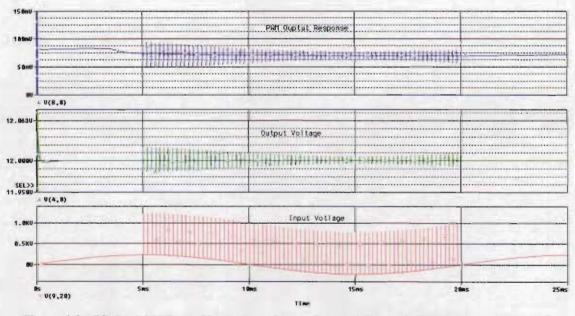


Figure 6-8 - PSpice 1 kV Burst Simulation - Input, Ouput voltages & PWM response zoomed

As the simulation waveforms show, the transient impulses reflected on the output are tiny (millivolts) compared to what is seen at the input. In the actual physical transient experiments, discussed in section 5.3.4, it was shown that transient phenomenon on the input to these types of circuits pass through the power supply into the appliance and appear at a much higher value than the output voltage. The transients recorded on the output of the power supplies were much greater than the very small transients recorded here in the simulations. The model represented in PSpice does not take into account stray capacitances and leakages that in reality are present in the actual power supply

circuitry. As a result the power supply's feedback circuitry is not as quick to take action to maintain the output as the simulation results yield.

6.3.3 Surge Immunity Simulations

In order to insert a surge onto the circuit input a voltage pulse was placed in series with the a.c. input source as shown in Figure 6-9.

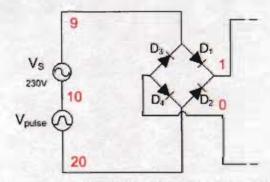


Figure 6-9 - PSpice circuit configuration for Surges generated on the Input

 V_S is the nominal 230 V a.c. 50 Hz sinusoidal source. The surge is generated by V_{pulse} set to occur at a certain time on the 50 Hz waveform.

```
VPULSE 10 20 PULSE(0 1570 25M 1.2U 100U 1N)
```

The pulse configuration file described a surge applied once on the positive peak of the sinewave and reaches a maximum of 1.8 kV. The characteristics used for the surge are determined from the EMC standard EN 61000-4-5. Here a rise time of 1.2 μ s with a fall time of 100 μ s is used.

The partial circuit file description for a 2 kV surge on the SMPS input is as follows:

Simulation waveform results for this surge test are shown in Figure 6-10 and Figure 6-11.

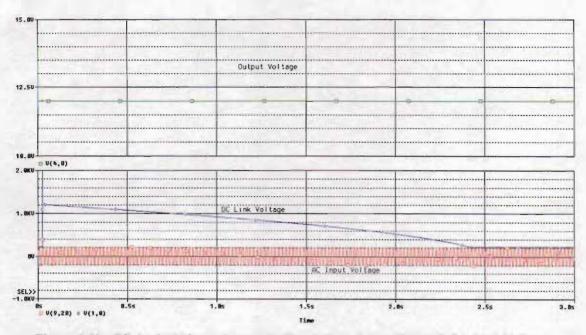


Figure 6-10 - PSpice 2 kV Surge Immunity Simulation - Input, Ouput & DC Link Voltages

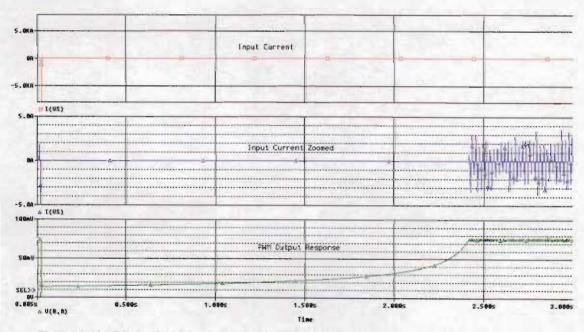


Figure 6-11 - PSpice 2 kV Surge Immunity Simulation - Input Current and PWM Output

The surge is applied during the second cycle's positive peak. It was noted from the simulation that the value selected for the input capacitor's ESR limited the voltage level seen on the d.c. link (output of the input rectification stage) after the initial application of the surge (see Figure 6-10). As can be seen from the waveforms this voltage charge across this capacitor takes approximately 2.4 seconds to return to its steady state. The control of the output is reflected in the pulse width modulator output waveform. The second figure also presents the input current response. At the surge there is an

approximate 8 kA spike in the current (which is very high and down to the choice of component values in the circuit). In practice varistor protection on the input to the power supply would limit the input voltage spike and current.

As the charge across the capacitor dissipates, the energy in the capacitor feeds the circuit and only when the voltage is back at steady state does the supply begin to draw current.

The output does not change throughout this disturbance and proves the circuit operates as expected. This is comparable to the physical tests discussed in section 5.3.5. The surges applied are of a longer duration than that of the transient bursts and the power supply circuitry were able to react fast enough to prevent the disturbance from reacting the output and entering the appliance circuitry.

6.4 Conclusion

The simulation results compared very well with the results obtained from the conducted EMC tests. Only one test proved to provide an inconsistency in the results. The transient bursts on the output of the SMPS were much more prevalent in the physical tests than in the simulation. This is due to inaccuracies in the PSpice model that does not take into account stray capacitances and leakages that are present in an actual circuit.

The PSpice software proved to be extremely useful in developing and simulating the switch-mode power supply model.

Chapter 7 Computer Modelling of Transient Disturbances in Medium Voltage Distribution Networks

7.1 The Electricity Network Grid

The electricity supply system (see Figure 7-1) is split into three main areas. The high-voltage (HV) transmission system consisting of 400/220/110 kV lines, feeds into the medium-voltage (MV) 38/20/10 kV distribution system, which in turn supplies the low-voltage (LV) 400 V (phase-to-phase)/230 V (phase-to-neutral) sub-distribution system. Generating stations across the country supply electrical power to the HV transmission network by means of overhead lines or underground cables. HV substations throughout the country use large transformers to transform the HV to MV. Industrial facilities which require this medium voltage can be fed from these transformers. Large facilities, e.g. Intel in Lexlip, may also have their own HV supply and use local substations to provide required voltage levels for use within the plant.

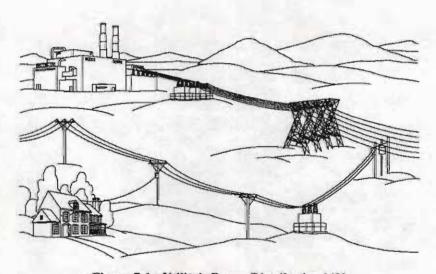


Figure 7-1 - Utility's Power Distribution [42]

At a more local level, for example a housing estate, there are transformers (pole mounted or ground mounted) that step down medium voltage to domestic low voltage. These transformers are configured in a delta/star winding configuration.

Typically the utility company will try to balance the loads put on each of the phases. Depending on the load demand, either a three phase and neutral (for larger commercial locations) or a single phase and neutral are used to supply a residence or multiple residences.

In the United States the domestic electrical system is different to most of the rest of the world in that they use a three-phase four-wire system with 208 V line-to-line and 120 V between phase and neutral at 60 Hz. This U.S. setup will have two phase conductors and one neutral conductor feeding the premises. Larger demanding loads such as water heaters, air conditioners, electric furnaces and cookers take supply from between the two phase conductors whereas smaller loads, lighting and those supplied through the wall power outlets etc. use the 120 V level. The electrical system configuration here incorporates everything being fed off a 230 V phase-to-neutral supply. Equipment which requires a different operating voltage from that supplied will include its own power supply to convert the voltage to the desired value (e.g. switch-mode power supplies).

Typically a residence would have a main utility installed fuse, a utility installed kWhr meter and a fuse or circuit breaker board at the entrance to the house. Figure 7-2 shows a simple schematic of this setup.

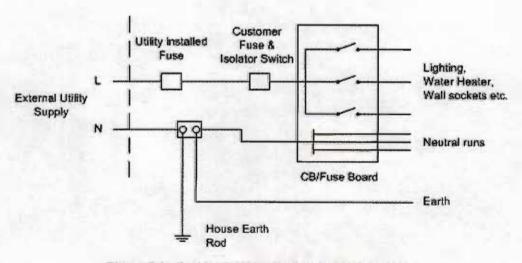


Figure 7-2 - Residential Distribution Board Schematic

The main utility fuse is used to protect the utility network from faults within the residence. The fuse or miniature circuit breaker board protects the consumer's equipment within the residence from internal system faults. These devices however generally only operate on electrical current overloads or short circuits to either blow the fuse or trip the breaker to make the related circuit safe. However these devices do not

provide protection against any form of nominal voltage variations, be it transients, surges, undervoltages or overvoltages.

And there usually is no other form of protection against these voltage occurrences on the utility company's MV or LV distribution system.

7.2 Surges on the network grid

Causes of surges in an electrical system can be attributed to one of the following [43]:

- Lightning
- · Opening and closing of switch contacts under load
- Switching of lightly loaded transformers
- · Severe load changes in adjacent systems
- Power line fluctuations and pulses
- Short circuits and blown fuses

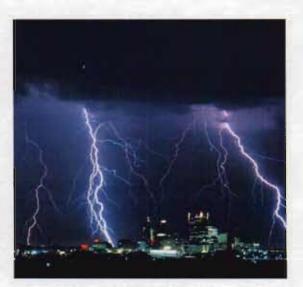
Lightning surges and switching surges are the two main disturbances that create great concern on the utility's network grid. Surges superimposed onto the network can be applied in two modes: "Common Mode" – across the live conductors and the earth conductor, "Differential Mode" – between various live conductors.

7.2.1 Lightning Surges

The natural phenomenon of *lightning* arises from charge separation in cumulonimbus clouds caused by meteorological conditions at the time, i.e. positive at the top of the cloud and negative at the bottom of the cloud.



Lightning seen across Dublin City during the recent storms of October 2003 (source: Irish Times newspaper)



Lightning storm over Oklahoma City [44]

Figure 7-3 - Lightning Images

Lightning is essentially a voltage source until it strikes a structure after which it becomes a current source. The maximum value of current from a strike can exceed 200 kA. There are many types of lightning which vary depending on geographical location. The most common form experienced is negative downward propagating lightning. Here a "leader" develops from the clouds (usually very high voltage – approximately 1 million volts) and a sharp point at the ground answers the leader and current is transferred. A typical current profile of a negative downward flash [45], shown in Figure 7-4, consists of 3 or 4 components. The first return stoke is followed by subsequent strokes that follow the plasma channel created (the easy path) and decreases in magnitude as the energy is taken from the cloud.

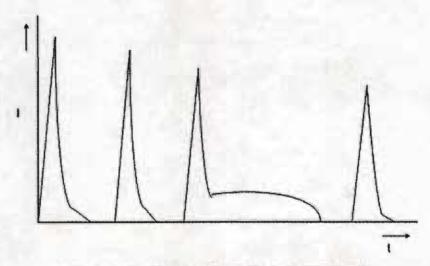


Figure 7-4 - Downward Negative Flash Current Profile

Positive downward propagating lightning strikes are another form of lightning. These are generally less common but however are experienced frequently in the west of Ireland due to weather fronts coming from the Atlantic Ocean. The downward positive flashes (see Figure 7-5) have longer rise-times and duration. This leads to higher peak currents leading to higher charge and energy transfer. It is unusual to have subsequent strokes with this type of lightning.

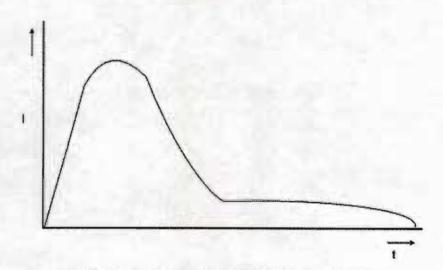


Figure 7-5 - Downward Positive Flash Current Profile

Table 7-1 gives an example of the electrical parameters of a downward propagating return stroke.

Parameter	Stroke Type	Probability Level		
		95 %	50 %	5 %
Peak Current [kA]	1 st Negative	14	30	90
	Subsequent negative	4.6	12	30
	Positive	4.6	35	250
Total Charge [C] $Q = \int i(t)dt$	1 st Negative	1.1	5.2	24
	Subsequent negative	0.2	1.4	11
	Positive	20	80	350
Energy [kJ/ Ω] $E = \int i(t)^2 dt$	1 st Negative	6.0	55	550
	Subsequent negative	0.55	6.0	52
	Positive	25	650	15000
Subsec	1 st Negative	9.1	24	65
	Subsequent negative	10	40	162
	Positive	0.2	2.4	32

Table 7-1 - Electrical Parameters of a downward return lightning stroke [45]

As can be seen the positive type has a tendency for higher energy transfer.

Upward Flashes occur at tall buildings with an upwardly propagating leader to the thunder cloud. They are very rare and only ever effect power systems with very tall overhead lines.

Direct lightning strokes (where it strikes the actual structure, overhead lines etc.) can reach a steepness of 100 kA/µs. These conducted surges can reach several hundred kilovolts. If the impact is on the MV network, the transmission of the surge through the MV-LV transformer takes place via capacitive coupling. As described in [46], a statistical study carried out in France showed that 91 % of lightning surges do not exceed 4 kV and 98 % do not exceed 6 kV at a LV consumer load. These findings are confirmed in the EN 61050 standard as described in the accompanying workbook.

Distribution lines are normally built at a lower height than transmission lines and are therefore less vulnerable to direct lightning strikes. They do, however, have no protection from direct lightning strokes in the form of shield wires as transmission lines do. Shield wires are basically an extra wire that runs above the transmission lines at the top of the pylons in order to intercept a lightning stroke and prevent it from striking the transmission conductors. The main hazard at distribution level is actually from indirect induced voltages in the overhead line during a nearby lightning flash.

Indirect lightning strokes (where the strike is nearby and affects installations in its vicinity) can cause a rise in the earthing potential when the lightning current flows through the ground. At a given distance, D, from the point of impact of the lightning the potential, U, is expressed by the equation: [46]

$$U = \frac{0.2 I \rho_x}{D} \tag{7-1}$$

where I = lightning current and $\rho_s = \text{ground resistivity}$.

The standardised lightning waveforms are the 1.2/50 µs voltage and 8/20 µs current waveforms as outlined in the EN 61000-4-5 surge immunity standard. As covered previously, characterisation of equipment according to this wave type is a reference for its lightning withstand capability.

7.2.2 Lightning Surge Models

As mentioned before and described in [46] lightning is described in terms of a current surge. Therefore to simulate a lightning surge on the network, a configuration of various Simulink tool blocks were used to produce both negative and positive downward propagating lightning. The waveforms created modelled those described by [45] and in [46]. These are shown in Figure 7-6.

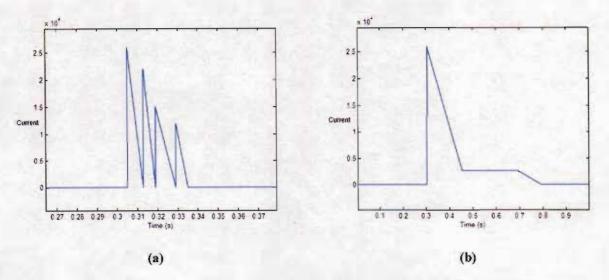


Figure 7-6 - Lightning Surge Waveforms (a) Negative (b) Positive

The configurations used for the negative downward lightning strokes are a 26 kA first pulse decaying over 8 ms, $50 \mu s$ later a 22 kA pulse for 6 ms, $50 \mu s$ later a third pulse of 15 kA over 10 ms and $50 \mu s$ after that a 12 kA pulse for 6 ms. The total time used for these lightning pulses is 30 ms.

Since positive lightning contains far much more energy and generally only exhibits one stroke the configuration used is as follows: 26 kA peak falling to 2.6 kA after 150 ms then after 240 ms it falls to zero after a further 100 ms. As noted by [45], these figures represent approximately 50 % of lightning strikes.

To simulate a 'worst-case scenario,' the same waveforms were used with values of 100 kA, 90 kA, 75 kA and 66 kA for the negative strokes and 210 kA, 21 kA for the positive stroke. These represent about 5 % of lightning strikes experienced in a year [45].

7.2.3 Switching Surges

These types of (man-made) disturbances occur when the network undergoes any rapid modifications, like the opening/closing of control and protection devices. Capacitor bank switching is a very common cause of these *switching surges*. Surges in a network with capacitors present propagate in the form of high frequency oscillating waves with rapid damping.

Switching surges are often also caused by sudden load changes on the network and even in the consumers own installation. The surge generated travels through the installations network to other connected loads.

The standardised waveforms [46] for switching surges are shown in Figure 7-7.

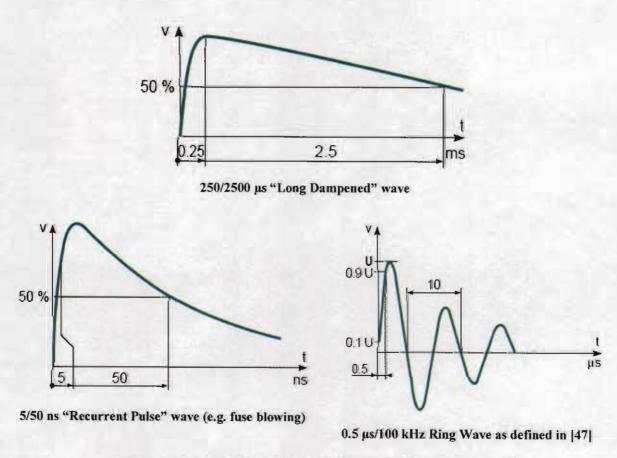


Figure 7-7 - Standardised Switching Surges representative waveforms

7.2.4 Surge propagation along transmission lines

The travelling wave theory describes the propagation of surges along transmission lines and cables. It is essential to understanding the behaviour of lightning and switching surges.

A transmission line can be described by its surge impedance (z_o) and transit time. For short lines and/or low frequency disturbances it can be modelled using one or more "PI-circuits" i.e. series resistance and inductance as well as a shunt capacitances as shown in Figure 7-8.

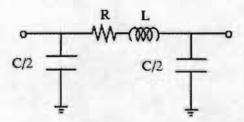


Figure 7-8 - PI Section representation of a Transmission Line

When a surge travels down the transmission line and meets a point of discontinuity i.e. another transmission line, transformer, load etc. which has a different impedance than that of the transmission line, there will be reflections and refractions or transmissions of the travelling wave at this point.

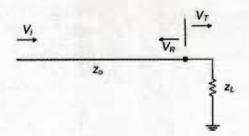
The speed of the propagation through the transmission line is given by

 $v = \frac{1}{\sqrt{LC}}$ [ms⁻¹] and in overhead lines is usually 3x10⁸ ms⁻¹ whereas for underground cables it is around half this.

The surge impedance (characteristic impedance) of a transmission line is given as

$$z_o = \sqrt{\frac{L}{C}} \tag{7-2}$$

At the point of discontinuity there will be a 'transmitted wave' and a 'reflected wave'.



Analysis shows,

$$V_{transmitted} = V_{incident} + V_{reflected}$$
 : $I_{transmitted} = I_{incident} - I_{reflected}$ (7-3)

... $\Rightarrow V_T = 2 V_i \frac{z_L}{z_o + z_L} = 2 V_i \beta_T$: $\beta_T = transmission coefficient$

Since $V_R = V_T - V_i$ this works out to

$$V_R = V_i \left(\frac{z_L - z_o}{z_L + z_o} \right) = V_i \beta_R$$
 : $\beta_R = reflection coefficient$ (7-4)

If the end of the transmission line is an open-circuit then $V_T = 2V_i$ and $V_R = V_i$ and the current transmitted must be zero. If it is a short circuit then the voltage transmitted must be zero and $I_T = 2I_i$ and $I_R = I_i$.

Using the above equations, the 'Bewley Lattice Diagram' can be used to determine the voltages and currents at points of discontinuity or at any point along a transmission network.

Figure 7-9 shows how the Bewley Lattice diagram may be used to determine the voltage at various points in a transmission network by adding transmissions and reflections in the diagram at the point of interest.

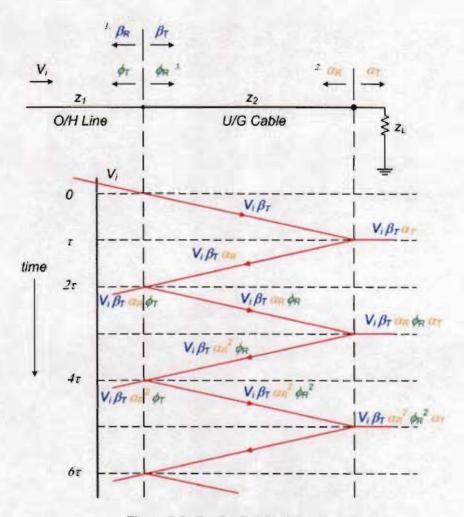


Figure 7-9 - Bewley Lattice Diagram

7.3 Medium Voltage Distributor Model

A network diagram of a typical medium-voltage distribution system was obtained from the ESB and a 20 kV MV feeder from this network was modelled using the Matlab Power System Blockset simulation package. The Tara E15 feeder chosen for the model is shown in Figure 7-10. A single line diagram representation of this feeder is shown in Figure 7-11.

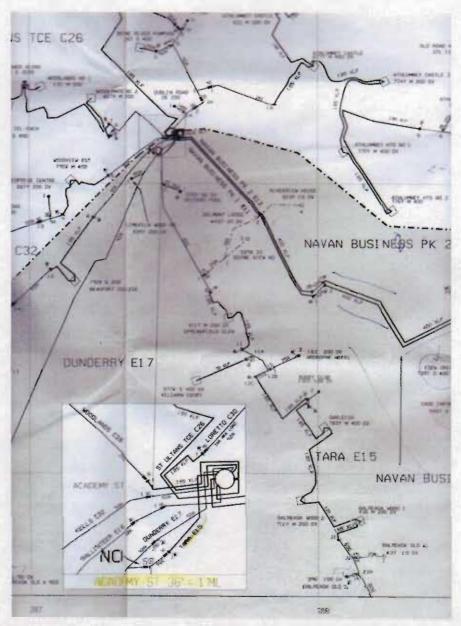


Figure 7-10 - ESB 20 kV Navan Tara E15 MV network diagram used as the basis for the computer model

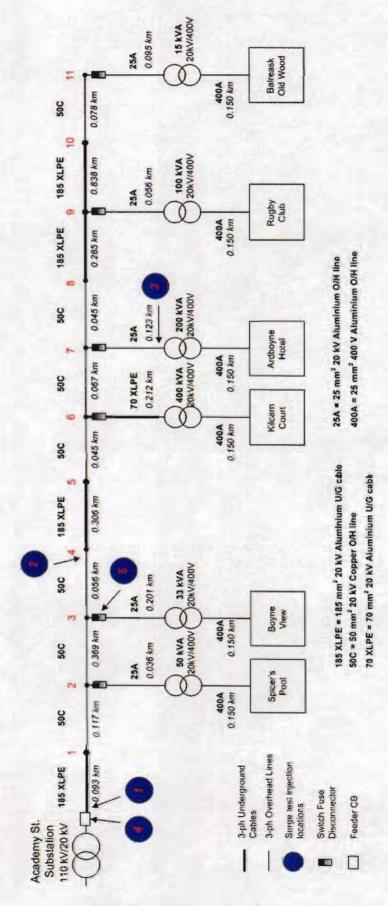


Figure 7-11 - One-line diagram representation of ESB MV network section Tara E15

Cable/overhead line types are presented on the diagram and the length calculated using the diagram scale. Information needed for the cable/line and transformer specifications were sourced from their manufacturing company ABB. Figure 7-11 also shows the injection locations of the surge simulation tests as described in Table 7-2 (see section 7.3.2 for further details).

The feeder consists of a number of underground cable and overhead line sections. These are as follows:

- 185 mm² XLPE 12.7/22 kV aluminium conductor single-core underground cables
- 70 mm² XLPE 12.7/22 kV aluminium conductor single-core underground cables
- 50 mm² Copper 20 kV overhead lines
- 25 mm² Aluminium 20 kV overhead lines
- 25 mm² Aluminium 400 V overhead lines

For each cable and overhead line section a nominal π -equivalent circuit, as shown in Figure 7-12, was developed using data obtained from the manufacturers ABB. The nominal π model was deemed to be sufficient because of the very short lengths of lines being considered.

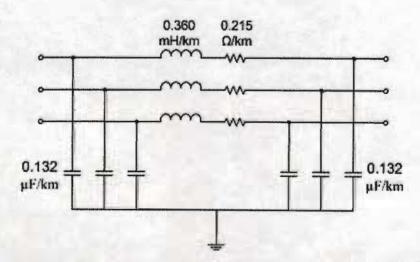


Figure 7-12 - 3-Phase transmission line equivalent π for the 185 XLPE underground cable

The parameters required from ABB were the resistance, inductance and capacitance values per km and these can be found in appendix H.

The three-phase delta/star transformers were modelled using the three-phase transformer model provided in the power system blockset. Additional capacitances,

from [48], were added to this model to account for interwinding and stray capacitances of the transformers.

On the LV side it was assumed that each transformer supplied an estate load through a short length of LV overhead line. As information on the LV network was unavailable a line length of 0.15 km was assumed. The LV lines were modelled using the nominal π -equivalent circuit discussed previously and the load on each transformer was set at 20 % of full-load at 0.9 power factor lagging.

7.3.1.1 Transmission Line model selection

Matlab PSB contains three models for transmission lines: distributed parameters lines, three-phase PI sections and single-phase PI sections. In order to determine which of these provides the most accuracy for the simulation, a switching-surge test circuit was created using each of these models, shown in Figure 7-13.

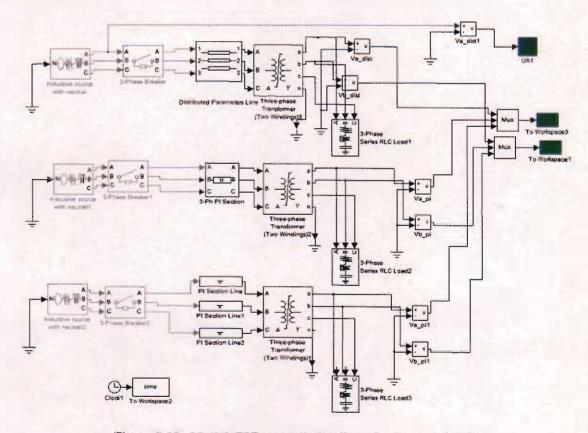
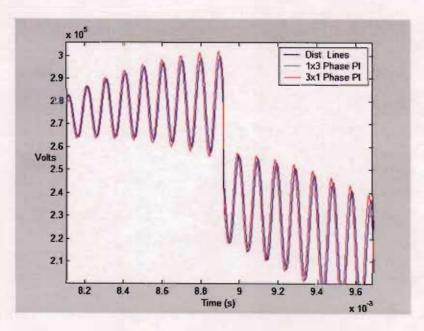


Figure 7-13 - Matlab PSB transmission line selection test circuit

A zoomed comparison of the response of the three different line models upon closing the feeder circuit breaker is shown in Figure 7-14. They exhibit close agreement with the two PI section tests showing exact correlation and the distributed parameters test yielding the same results with a very slight phase shift. A section of the network feeder model was then subjected to a negative lightning disturbance using each of the transmission line models (the source feed up to and including the Boyne View tap-off). Arising from this the total time for the full network simulations became a clear consideration. The distributed parameters lines test took over 2 days to simulated just 0.6 seconds and proved to be a great stress on the PC system. The three-phase PI section test took over an hour to simulate the same time and using single-phase PI sections on each phase only took approximately 30 seconds.

Therefore from this, and considering the total simulation time for a full simulation, it was concluded that using single-phase PI sections represents an appropriate model for the transmission lines. Also, the distributed parameters lines are generally recommended for modelling long transmission line runs and since the lengths for this network model are short the PI sections prove more adequate. Most of the full network simulations took many hours so the simulation time savings using the single-phase PI sections was highly beneficial.



The red single-phase PI section line completely masks the green three phase PI section line.

Figure 7-14 - Transmission line model selection comparison

7.3.2 Simulation Tests

On completion of the Matlab line model a number of events were simulated to assess their impact on the LV side of the consumer transformer. In particular, Table 7-2 lists the events that were simulated.

	Test Description	Location on the Feeder (see Figure 7-11)
Test 1	a) 26 kA Negative Lightning injected at the feeder source b) 100 kA Negative Lightning injected at the feeder source	1
Test 2	a) 26 kA Negative Lightning injected at the feeder source with surge arrestors b) 100 kA Negative Lightning injected at the feeder source with surge arrestors	1
Test 3	a) 26 kA Negative Lightning injected on the line b) 100 kA Negative Lightning injected on the line	2
Test 4	a) 26 kA Negative Lightning injected on the line with surge arrestors b) 100 kA Negative Lightning injected on the line with surge arrestors	2
Test 5	a) 26 kA Positive Lightning injected at the feeder source b) 210 kA Positive Lightning injected at the feeder source	1
Test 6	a) 26 kA Positive Lightning injected at the feeder source with surge arrestors b) 210 kA Positive Lightning injected at the feeder source with surge arrestors	1
Test 7	a) 26 kA Positive Lightning injected on the line b) 210 kA Positive Lightning injected on the line	2
Test 8	a) 26 kA Positive Lightning injected on the line with surge arrestors b) 210 kA Positive Lightning injected on the line with surge arrestors	2

Test 9	a) 26 kA Negative Lightning injected at Ardboyne Hotel b) 100 kA Negative Lightning injected at Ardboyne Hotel	3
Test 10	a) 26 kA Negative Lightning injected at Ardboyne Hotel with surge arrestors b) 100 kA Negative Lightning injected at Ardboyne Hotel with surge arrestors	3
Test 11	Opening and closing operation of feeder CB	4
Test 12	Opening and closing operation of feeder CB with surge arrestors	4
Test 13	Operation of an overhead switch fuse disconnector at Boyne View	5
Test 14	Operation of an overhead switch fuse disconnector at Boyne View with surge arrestors	5

Table 7-2 - Surge simulations tests

It should be noted that the right hand column of Table 7-2 is referring to Figure 7-11 as well as Figure 7-15 and shows the location in the line at which the event occurred e.g. Test 1 was a 26 kA lightning surge injected at the feeder source.

Tests 1 to 8 simulated the injection of lightning surges at various points along the feeder. Two types of lightning surges were injected; a) 26 kA lightning representing a probability of 50 %, b) 100 kA/210 kA, the 'worse-case scenario' representation, as discussed in section 7.2.2. All lightning surges were applied between phase A and earth. Tests 9 and 10 were carried out to see how a direct strike at the Ardboyne Hotel load spread through the line. Tests 11 and 12 simulated switching surges by opening and closing the feeder circuit breaker. Tests 13 and 14 simulated the operation of a switch fuse disconnecting isolator at Boyne View estate. The closing of the switch fuse disconnector is simulated. It is assumed that during the closing operation contact bounce occurs resulting in multiple breaking and making of the switch contacts. This process is modelled using ideal switches controlled by timers. The reason for performing this test is to reproduce what might occur when an estate is reconnected after being isolated for maintenance or repair work.

Figure 7-15 shows the full power system blockset model for the Tara E15 MV distributor. Measurements of voltage and current are recorded at various points on the line and at the HV and LV sides of each consumer transformer (the green boxes indicate the measurement points). The MV/LV transformer and the loads are masked under the orange blocks, the contents of which are shown in Figure 7-16.

A second version of the above model was also developed which included surge arrestors (rated for 75 kV) at the HV side of the consumer transformers as this would allow comparisons to be made for systems with and without surge arrestors installed. Surge arrestors installed at the transformers are used to limit the voltage appearing at its input by diverting a portion of the surge, above their rated value, to earth. Utility companies generally do not install surge arrestors at these pole/ground mounted transformers. They may install them in areas that are highly prone to surge disturbances however.

The tests in Table 7-2 were carried-out at no load, light loading and full load conditions of the MV/LV transformers.

The disturbances were injected 305 ms into the simulation, at the positive peak of the input voltage. Simulation time lengths varied with the simulations being run.

Using the plot function of Matlab the waveforms captures were extracted and saved. The peaks reached were recorded and tabulated. Full results can be found in appendix I.

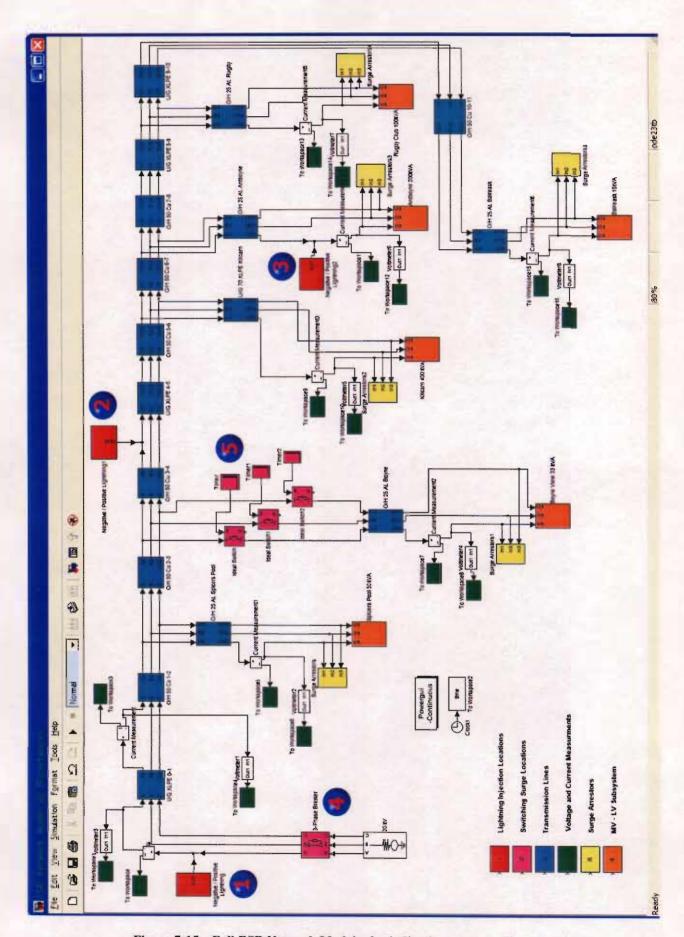


Figure 7-15 - Full ESB Network Model: also indicating surge application points

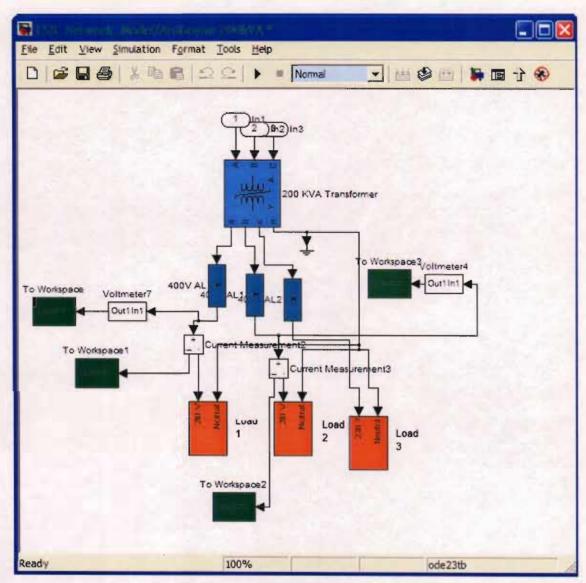


Figure 7-16 - MV-to-LV Network Section

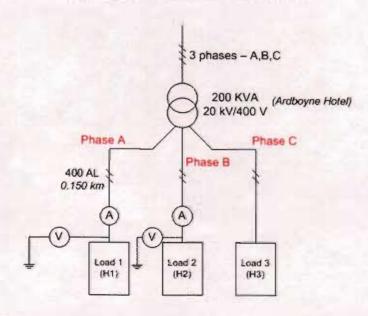


Figure 7-17 - Low voltage level single line diagram representation of Figure 7-16

Figure 7-17 shows the single line diagram representation of the Matlab PSB constructed model of the low-voltage side of the network feeder model, as shown in Figure 7-16. Information on this low voltage section was not provided by ESB so the model used is assumed. The example shown is the Ardboyne Hotel 20 kV/400 kV MV transformer and LV side connections. Each estate is similar however the ratings are changed as appropriate, as seen in Figure 7-12. Each phase and corresponding neutral feeds a load (depicted using the abbreviations H1, H2 and H3). The current and voltage at loads H1 and H2 are monitored. Most of the disturbances are injected on phase A so phase A on the LV side is monitored to see the effect they have at the connected load and phase B is also monitored to see the effect the disturbances have on the other phases as it passes through the transformer.

7.3.3 Simulation Results and Discussion

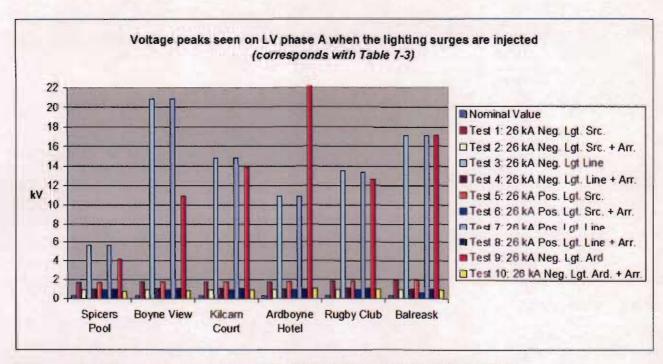
The simulations yielded well over 1,400 voltage and current waveforms to be consulted. For each test completed, surge voltage and current peaks were tabulated. Table 7-3, Table 7-4 and Table 7-5 show results obtained at the LV side of the transformers. Figure 7-18, Figure 7-19, Figure 7-20 and Figure 7-21 provides a graphical view of the lightning simulation results contained in these tables for each test at the individual LV loads. Full results are contained in appendix I.

The tables show the voltage and current peaks reached at the H1 and H2 loads at each estate for the various tests performed. For example, *VspicerH1* refers to the voltage level reached on phase A at the Spicer's Pool estate as shown in Figure 7-11. *IspicerH1* is the current recorded on this phase. *VspicerH2* and *IspicerH2* refer to measurements on phase B etc. They are presented in progressive order along the feeder line.

Test 13	Sw Surge Fuse	_	0.794 kV	1	18	AND COLUMN	0.363 kV		1	-0.533 kV	1	1	1	1		1	1	1	1	1	/		-	1	1	1	1
Test 12 & 14	Sw Surge Src + Fuse Arr	ARR.'S		DO NOT		EXCEED			ARR.'S		RATING	141							100								
Test 11	Sw Surge Src		1	1	1	1	1		0.52 kV	0.56 kV	0.54 kV	0.583 kV	0.565 kV	0.604 KV		1	1	1	1	1	1	27.6A	1	1	1	1	1
Test 10	26kA Neg. Lgt Ard+Arr	0.832 kV	0.89 kV	0.962 kV	1.13 kV	118	0.98 kV		0.579 kV	0.601 kV	0.617 kV	0.62 kV	0.618 kV	0.619 kV		57.15 A	27 A	340 A	182 A	86.5 A	13 A	39.8 A	16 A	200 A	99.5 A	50 A	74A
Test 9	26kA Neg. Lgt Ard	4.18 KV	10.87 kV	13.9 kV	47 kV	12.6 kV	17.1 kV		0.619 kV	2.18 kV	2.74 KV	2.75 kV	-3.71 kV	4.76 KV		276.5 A	138 A	2160 A	3400 A	494 A	97.3A	41.5A	30 A	444 A	220.5 A	132 A	24.8 A
Test 8	26kA Pos. Lgt Line+Arr	1.01 kV	1.13 KV	1.09 kV	1.05 kV	1.09 kV	0.995 kV		0.651 kV	0.685 kV	0.706 kV	0.708 kV	0.706 kV	0.706 KV	-107011	88.89	29.1 A	325.9 A	176 A	88.2A	13.2 A	44.6A	17.3A	221 A	111 A	55.2 A	84A
Test 7	26kA Pos. Lgt Line	5.61 kV	20.9 kV	14.8 kV	10.9 kV	13.4 kV	17.1 kV		0.647 kV	0.693 kV	0.738 kV	0.705 KV	0.715 kV	0.76 kV		309 A	254 A	2230 A	869 A	521 A	96.7 A	44.5A	17.A	217 A	108 A	54 A	8.15A
Test 6	26kA Pos. Lgt Src+Arr	VA 66.0	0.955 kV	0.955 KV	0.955 kV	0.955 KV	0.617 kV		0.668 kV	0.668 kV	0.668 kV	0.668 kV	0.668 kV	0.668 kV		67.8 A	28.6 A	343 A	172A	86.1 A	13.2A	38.48 A	16.5 A	206 A	103 A	51.4 A	7.75A
Test 5	26kA Pos. Lgt Src	1.71 kV	1.82 kV	1.76 kV	1.76 kV	1.83 kV	1.94 KV		0.612 kV	0.666 kV	0.666 kV	0.666 kV	VM 999.0	0.666 kV		94.8A	32.5 A	393 A	197 A	98.8A	15.2A	42 A	16.8A	214 A	107 A	53.3 A	8 A
Test 4	26kA Neg Lgt Line-Arr	1.01 kV	1.13 kV	1.09 kV	1.05 KV	1.09 kV	0.994 kV		VX 672.0	0.598 kV	0.61 kV	0.612 kV	0.61 kV	0.61 kV		68.8 A	28.8 A	350 A	175 A	88 A	13.2 A	39.5A	16.7 A	210 A	105 A	52.5 A	79.A
Test 3	26kA Neg. Lgt Line	5.61 kV	20.9 kV	14.8 kV	10.89 kV	13.5 kV	17.1 kV	-	0.74 kV	2.48 kV	2.87 kV	2.89 kV	-3.52 KV	4.74 KV		309 A	254 A	2230 A	866 A	521A	96.6 A	49 A	34.1A	464 A	234 A	125 A	252 A
Test 2	26kA Neg. Lgt Src+Arr	0.988 kV	0.953 kV	0.94 KV	0.936 KV	0.94 KV	0.947 KV		0.56 KV	0.59 kV	0.59 kV	0.59 kV	0.589 KV	0.59 kV		67.8 A	28.6 A	343 A	172A	86.1 A	13.26	38 48 A	16.5 A	206 A	103 A	51.4A	7.75A
Test1	26kA Neg. Lgt Src	1,709 KV	1.816 KV	1.756 kV	1.75 kV	1.825 KV	1.93 kV		0.56 kV	0.58 kV	0.592 kV	0.593 kV	0.592 KV	0.59 kV		94.5A	32 A	382 A	192 A	97.5A	152A	385A	164A	205 A	103 A	51A	7.7 A
	Nominal Peaks	0.325 kV	0.325 kV	0.325 kV	0.325 KV	0.325 KV	0.325 KV	100000000000000000000000000000000000000	0.325 KV	0.325 kV	0.325 kV	0.325 kV	0.325 kV	0.325 kV		22 A	13.2 A	160 A	80 A	40 A	6A	22.A	13.2A	160 A	80 A	40 A	6.A
	Light Loading	VspicerH1	VbowneH1	VkilcarnH1	VardH1	VrugbyH1	VbalH1		VspicerH2	WoowneH2	WeilcarnH2	VardH2	VrugbyH2	VbalH2	10.00	IspicerH1	IboyneH1	IkilcarnH1	lardH1	IruqbyH1	lball1	SpicerH2	lbowneH2	IkilcarnH2	lardH2	IruqbyH2	lbalH2

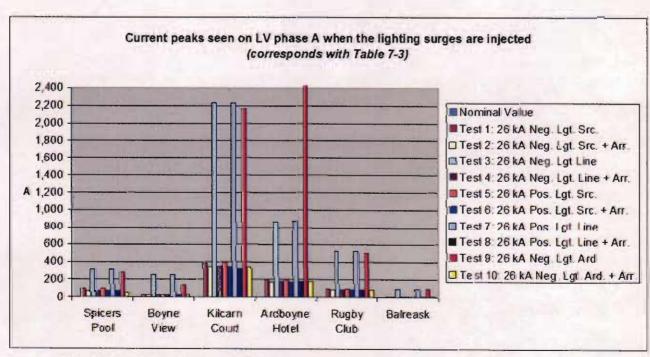
Table 7-3 - Simulation Results for light loading and 26 kA lightning: shows the voltages and currents at the LV consumer level

H1=LV Phase A load H2=LV Phase B load



(Note: Test 9 at Ardboyne Hotel reaches 47 kV but graph is cut-off at 22 kV for presentation purposes)

Figure 7-18 - Graphical representation of phase A voltage peak results from Table 7-3



(Note: Test 9 at Ardboyne Hotel reaches 3,400 A but graph is cut-off at 2.4 kA for presentation purposes)

Figure 7-19 - Graphical representation of phase A current peak results from Table 7-3

hase A

		Test1	Test 2	Test 3	Test 4	Test 5	Tsst 7	Test 8	Test 9	Test 10	Test 11	14	Test 13
Light Loading	Nominal Peaks	100kA Neg. Lgt Src	100kA Neg. Lgt Src+Arr	100kA Neg. Lgt Line	100kA Neg. Lgt Line•Arr	Pos. Lgt Src	210kA Pcs. Lgt Line	210kA Pos. Lgt Line+Arr	100kA Neg. Lgt Ard	100kA Neg. Lgt Ard+Arr	Sw Surge Sre	33	Sw Surge Fuse
VspicerH1	0.325 KV	5.78 kV	1.17 kV	20.8 kV	112kV	11.9 kV	45.4 KV	1 18 KV	12.7 kV	0.883 kV			
WhoymeH1	0.325 kV	6.21 KV	1.03 KV	79.5 kV	125 kV	12.8 kV	17 KV	1.3 kV	41 KV	0.947 KV			
WilcarnH1	0.325 kV	5.98 KV	0.996 kV	562 KV	1.18 KV	12.3 kV	117.7 kV	126 kV	48.9 KV	1.01 kV			
VardH1	0.325 KV	5.86 kV	0.985 kV	39.4 kV	1.17 kV	12.3 kV	82.5 KV	123KV	180.3 kV	1.23 kV			
VrugbyH1	0.325 KV	6.25 KV	0.98 KV	42.8 kV	1.2 KV	12.8 kV	8£.7 kV	127 KV	40.6 kV	1.03 kV			
VbalH1	0.325 KV	6.65 kV	0.973 kV	65 kV	1.17 kV	13.7 kV	1:7 kV	1.15 kV	65.1 kV	1.01 kV			
VspicerH2	0.325 KV	1.04 kV	0.738 kV	3.47 KV	0.773KV	1.39 KV	437 KV	0.786 KV	3.76 kV	0.704 kV			
VboymeH2	0.325 kV	1.39 KV	0.805 kV	9.43 kV	0.835 kV	229 kV	1£1 kV	0.859 kV	10.9 KV	0.789 kV			
VkikarnH 2	0.325 KV	1.63 kV	0.849 kV	11.5 kV	0.89 kV	2.82 kV	17.3 KV	0.91 kV	14.5 KV	0.846 kV			
VardH2	0.325 KV	-1.47 kV	0.852 kV	112 kV	0.89 KV	2.9 kV	18 KV	0.911 KV	15.7 KV	0.861 kV			
VrugbyH2	0.325 kV	1.78 KV	0.85 kV	14.5 kV	0.89 KV	3.06 kV	2C.8 KV	0.91 kV	19 kV	0.854 kV			
VbalH2	0.325 kV	1.94 kV	0.852 kV	19.4 KV	0.89 kV	3.48 kV	24.5 KV	0.908 kV	24.4 KV	0.855 kV			
snicerHf	A 00	309 8 A	RO A	1130 A	75.5 A	633 A	2 160 A	79 E.A	833 A	607A			
lboyneH1	13.2 A	86. A	30.3 A	\$41.A	31.7 A	167.A	1.60 A	329A	493. A	27.5 A			
IkilcarnH1	160 A	1,005. A	359. A	8,130.A	378.A	1,950.A	16300.A	391 A	7,140.A	351. A			
lardH1	80 A	502.A	178. A	2,870. A	186.A	971.A	5,40.A	188.6A	12,900. A	198.3 A			
rugbyH1	40 A	264. A	89. A	1,560. A	93. A	514.A	3,140.A	92. A	1,500.A	89. A			
lbalH1	6A	41.8 A	132 A	355. A	13.4 A	81.5A	636. A	13.1 A	358. A	13.A			
IspicerH2	22.A	714A	51.A	233.A	53. A	94.5A	313. A	53.8 A	257.A	48.4 A			
lboyneH2	13.2A	20.4 A	18. A	112.A	18. A	29.3 A	1'6.A	17.8 A	127.4 A	172A			
kilcarnH2	160 A	282.5A	233. A	1,660. A	235. A	416.8A	2,480.A	233.A	2,060. A	222 A			
lardH2	80 A	144.A	117. A	810.A	118 A	219.A	1,90.A	116.2A	1,120.A	110.A			
IrugbyH2	40 A	73.6A	58.4 A	517. A	585A	119.A	715. A	57.7 A	679. A	55.3 A			
Mall	V J	442 A	V 0 0	A CAL	V 0 0	1 4 4 40	430.6	4 6 0	4 000	4 000			

Table 7-4 - Simulation Results for light loading and 100/210 kA lightning: shows the voltages and currents at the LV consumer level

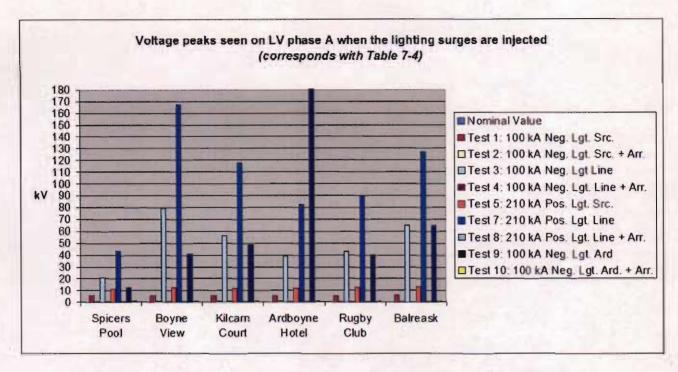
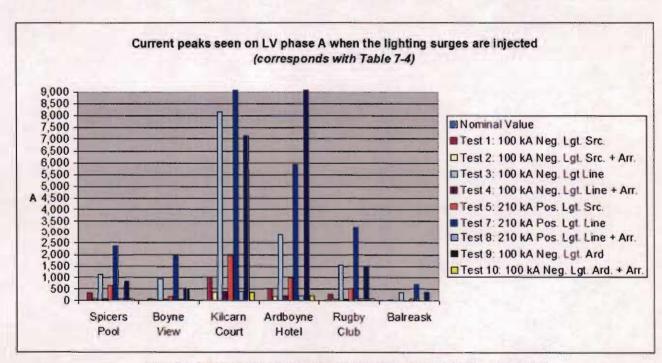


Figure 7-20 - Graphical representation of phase A voltage peak results from Table 7-4



(Note: Test 7 at Kilcarn Court reaches 16.9 kA and Test9 at Ardboyne Hotel reaches 12.9 kA however the graph is cut-off at 9 kA for presentation purposes)

Figure 7-21 - Graphical representation of phase A current peak results from Table 7-4

Test 13	Sw Surge Fuse	-0 540 KV	10.7 kV	0.344 RV	0.353 kV	0.362 KV	0.402 kV		63 kV	1	d	1		1	160 A					-	-96A	1	1			
Test 12 & 14	Src																	I								
Test 11	Sw Surge Src																									
Test 10	26kA Neg. Lgt Ard+Arr		0.00					SULUE IN THE SECOND																		
Test 9	26kA Neg. Lgt Ard																									
Test 8	26kA Pos. Lgt Line+Arr			~						000					~	2500										
Test 7	26kA Pos. Lgt Line			LOADING OF THE TRANSFORMER		FECT ON		TIRRENT				UTPUTS			LOADING OF THE TRANSFORMER		FECT ON	1000	UKKENI				UTPUTS			
Test 6	26kA Pos. Lgt Src+Arr			THETRA		E TO NO E		THE VOLTAGE AND CLIRBENT		PEAKS	3	SEEN ON THEIRS OUTPUTS			THETRA		E TO NO E		THE VOLI AGE AND CORREN	ſ	PEAKS		SEEN ON THEIRS OUTPUTS			tion
Test 5	26kA Pos. Lgt Src			JADING OF		HAS LITTLE TO NO EFFECT ON		THE VOLT				SEENON			DADING OF		HAS LITTLE TO NO EFFECT ON		INE VOLI	Ī			SEENON			/=no deviation
Test 4	26kA Neg Lgt Line+Arr			ï				Ī	Ī	Ī				ĺ	10	ï										
Test 3	26kA Neg. Lgt Line	5.6 kV	100%					738 V						309/22												ase A load
Test 2	26kA Neg Lgt Src+Arr		SAME		AS		WITH		HGHT		COAD				SAME		AS		WIII		LIGHT	THE REAL PROPERTY.	LOAD			H1 = LV Phase A load H2 = LV Phase B load
lest 1	26kA Neg. Lgt Src		SAME		AS		WITH		THE		DAD				SAME		AS		WIIH		LIGHT	0.00	LOAD			
	Nominal Peaks	0.325 kV	0.325 KV	0.325 KV	0.325 kV	0.325 KV	0.325 kV	U 305 bV	0 325 kV	0 325 kV	0.325 kV	0.325 kV	0.325 kV		13.2.A						132A					
	Full	VspicerH1			VardH1	VrugbyH1	н	Venicortty			100	-		IspicerH1	IboyneH1	IkilcarnHi	lardH1	IrugbyH1	IDaH11	chicorh?	lboyneH2	IkilcarnH2	lardH2	IruqbyH2	IbaH12	

Table 7-5 - Simulation Results for full loading and 26 kA lightning. *Note*: Test 13 was the only test to show different results

7.3.3.1 Results Test 1 and 2: Negative and Positive Downward Lightning at the feeder source (pt. 1)

As can be seen in the tables on the previous pages, when the 26 kA surge is injected onto phase A of the network it propagates along the line.

The voltage levels reached at the LV loads on the phase A output of the transformers (H1 entries in the table) show that for a negative lightning 26 kA surge (50 % of lightning that is experienced) injected at the output of the Academy Street substation, the voltage levels do not exceed 2 kV, which is the limit set down in the EN 61000-4-5 standard to which domestic appliances should be built to withstand. Through the winding connections of the transformer the surge effects are also seen on the other phase outputs of the transformer (H2 entries for phase B), although they do not reach any significant level. These voltage surges are those associated with the injected current surge. A corresponding current surge also reaches the loads. The surge levels however would be distributed between the houses that are fed off the phases. It would then be distributed further throughout the circuit branches within a house to which the domestic appliances are powered. The general duration of the surge peaks experienced are approximately 2 ms. A typical domestic fuse current-time characteristic shows that a current magnitude of at least 2 kA would melt the fuse element at this length surge duration. Therefore the current surges experienced during this simulation, which are all about 2.4 times the peak during steady-state, would pass through these fuses and into the residences, where it would also pass through the fuse and circuit breaker protections on the domestic circuit branches. Each branch will experience the surge at a lesser value than it was at when it entered the estate. However, if a piece of sensitive equipment sees a high portion of this current surge its components may be damaged e.g. a personal computer is rated for approximately 1.5/3 A and if a high proportion of the 382 A surge, as seen on phase A at Kilcarn Court, appears at the power supply of the PC, its components could be damaged. The duration of the surge at this point determines the energy delivered and this will also determine if damage or malfunction will result.

The effects of *installing surge arrestors* on the primary side of the MV/LV transformers are seen in the next column. Surge arrestors are generally not installed by the utility company at this point as they are expensive and bulky to fit. They may be installed in areas that experiences high levels of surges. It is clear that the surge arrestors reduce the

voltage level seen at the residence significantly; however the current surges are only decreased to a factor of 2.2. As outlined previously, the high current level seen could play a part in upsetting an appliance.

The tables also show that the same values are reached for the *positive lightning* simulations of the same peak amplitude. However, since the actual positive surge contains a lot more energy and lasts for a longer time than the negative lightning (see Figure 7-6) it has an overall greater effect when it reaches the LV loads.

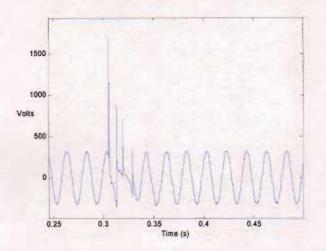
Figure 7-22 shows sample waveforms from these simulations discussed, for both the negative and positive downward lightning simulations. Voltage and current recordings are shown at Spicers Pool (the first branch of the line) and at Kilcarn Court (further down the line). For negative lightning the effect of the four impulses are clear to see whereas the characteristic of the positive lightning conveys a different result.

As can be seen from the figures, the positive lightning's effects are greater and longer. After the surge peak, a sag is experienced. This gradually recovers over the time it takes for the positive lightning surge peak to decay to where it remains constant at 2.6 kA. Here the voltage and current returns to its steady-state sinusoidal characteristic.

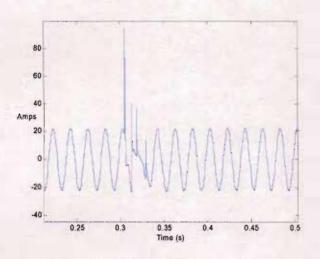
The sag experienced however lasts for 150 ms (7.5 cycles). If the surge peak did not upset an appliance the sag may do if the duration and amplitude experienced are larger than the values used here (positive lightning surges can commonly last up to 0.9 seconds). As shown from the physical experiments in Chapter 5, a voltage dip of 40 % in the region of 500 ms can cause disruption to personal computer operations.

When the current peaks at Spicers Pool and Kilcarn Court are compared it is evident that some of the surge energy has been attenuated as it travelled through the line. The peak values seen are different and this is dependent on the transformer ratings, however the ratio of the peak to the nominal peak reached is significantly reduced at Kilcarn Court.

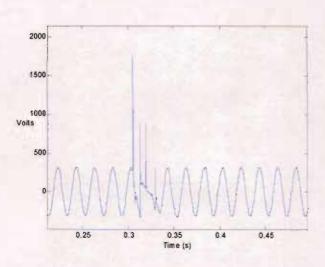
Negative Lightning at point 1



(a) Voltage at Spicers Pool on phase A

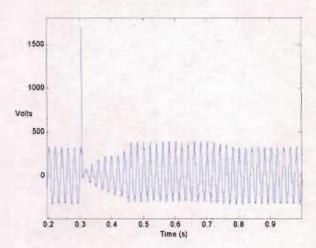


(c) Current at Spicers pool on phase A

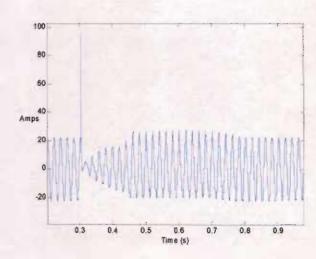


(e) Voltage at Kilcarn Court on phase A

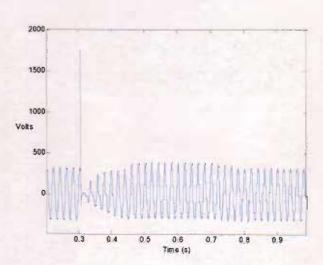
Positive Lightning at point 1



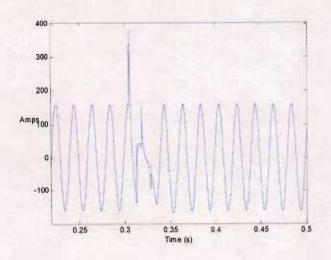
(b) Voltage at Spicers Pool on phase A

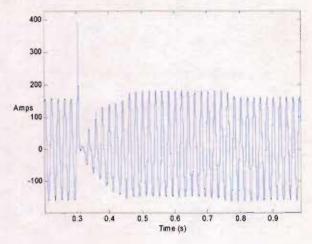


(d) Current at Spicers pool on phase A



(f) Voltage at Kilcarn Court on phase A





(g) Current at Kilcarn Court on phase A

(h) Current at Kilcarn Court on phase A

Figure 7-22 - Voltages and Currents reaching houses on phase A at Spicers Pool estate and Kilcarn Court

7.3.3.2 Results Tests 3 and 4: Negative and Positive Downward Lightning at pt. 2

The same surges were applied to phase A at the point where the transmission through an underground cable meets overhead lines (point 2 in Figure 7-15). As can be seen from the test results tables the levels of voltages and currents reached at the various transformer outputs for both lightning types are much greater than the results previously discussed.

These levels are sure to damage appliances in the houses. However, the voltage levels seen on the primary of the transformers are so high that it is likely insulation failure or flashover will occur and cause the feeder circuit breaker to trip and the loads to lose power. The simulation does not account for this action and hence the results obtained should be treated cautiously.

Installing surge arrestors again plays a significant part in protecting the transformers and those connected on their outputs. As shown, the input voltages entering the transformers are restricted in the region of 84 kV which in turn provides an output voltage peak of around 1 kV.

7.3.3.3 Results: 100 kA Negative - 210 kA Positive Lightning simulation results

Tests 1 to 4 were repeated at the lightning surge values to those depicted by [45] as being less than 5 % of lightning strikes experienced.

The results in Table 7-4 show that the levels experienced on the transformer outputs are indeed much greater than the lower lightning surge values. The high voltages and currents would certainly cause damage and upset to appliances in the houses. Even residents on phases B and C experience high levels of the disturbance and would also be affected. Again these results would have to be treated with caution as it is likely that insulation breakdown in the MV network would occur and cause the network to lose power. It can not be clear how much of the disturbance reaches the LV side before the breakdown occurs.

Again the surge arrestors play a part in protecting the transformer and loads connected. The surge arrestors would most probably have been damaged as a result of these surges, thus leading to costly replacements.

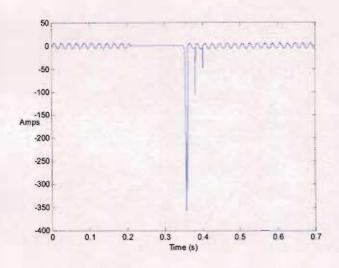
7.3.3.4 Results Tests 9 and 10: Lightning at Ardboyne Hotel

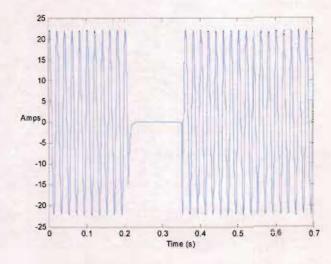
The same conclusions can be drawn from the results seen when lightning strikes at the transformer feeding Ardboyne Hotel. Extremely high voltages and currents are sent throughout the network which would result in certain insulation breakdown thus tripping out the MV network.

7.3.3.5 Results Tests 11 to 14: Switching Surges

The switching surge simulations did not produce such problematic results as the lightning simulations. Two switching events were simulated. (a) The opening and closing of the feeder circuit breaker, (point 4 in Figure 7-15). The circuit breaker switches out the network and 145 ms later re-closes. (b) The closing of the switch fuse disconnector at Boyne View, taking into account multiple restrikes at slightly different times on each phase.

Example waveforms from both simulations are shown in Figure 7-23 and Figure 7-24.



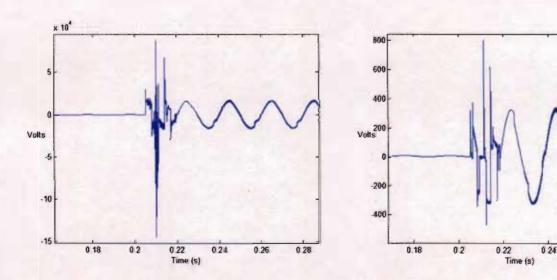


- (a) Current at Spicer Pool transformer primary
- (b) Current on phase A of the transformer output

0.26

0.28

Figure 7-23 - Switching Surge simulation at point 4: Current waveforms at Spicers Pool



(a) Voltage at Boyne View transformer primary (b) Voltage seen on phase A output of the transformer

Figure 7-24 - Switching Surge simulation at point 5: Voltage waveforms at Boyne View

As can be seen from the various results and the waveforms, the operation of the circuit breaker does not produce voltage or current surge transients on the output of the transformers. Phase B did experience some minor peaks, but these would not have any affect on the consumer's appliances. The transformer winding connections also play a significant part in damping the surges.

The system loading did not have any influence on the peak values seen at the transformer LV terminals.

The closing of the switch fuse disconnector simulation at the feed into the Boyne View estate when lightly loaded also did not produce any results to be concerned about. The Boyne View estate was obviously the most effected. As its power was being restored, as Figure 7-24 shows, there is a transient response seen at both the primary and output of the transformer. The peak value reached is only 793.5 V and this level of surge would not upset domestic appliances.

Fully loading the transformers on the network however did have an affect on the results of this simulation. Excluding the Boyne View tap-off, all other feeds did experience a minor surge at both the input and output of the transformers. However, their values were not high enough to be of concern. The Boyne View estate when fully loaded did however see a dramatic increase in the surge levels on the transformer input and at the loads connected to it; 10.7 kV and 6.3 kV are seen on phases A and B respectively at the consumer loads. This level of surge (with duration 0.9 ms) would certainly result in domestic appliances being damaged or upset.

This however is considering the appliances are left switched on during the power outage. This is the reason it is recommended that electricity users switch off all electronic equipment when a power outage is experienced. This would reduce the load on the network when the power is restored and, as can be seen from the results obtained here, would decrease the risk of resulting damage.

7.3.3.6 Additional Comments on the results

Simulations of the model at full load and no load proved to have little effect on the lightning surge results when compared to that of the lightly loaded case. The only test where the loading of the transformers became an important issue is when the voltage was being restored to a particular transformer. Here the increased loading induced a higher surge at the loads.

7.4 Conclusion

From the simulations of the MV distributor it is clear, as expected, that the level and severity of the surges experienced at the LV consumer loads depends on the location of the load in relation to the injection point were the lightning surge is applied. The MV/LV transformers play a part in suppressing the surge; however the surge magnitude that appears on their output depends on the level seen at the input. When the surge that is injected on phase A passes through the transformer, it is seen on the other two output phases but at a much lower value than on phase A. Installing surge arrestors can limit the surge levels experienced at the transformer inputs and outputs.

The more common strength of lightning (50 %) produced surge levels at the LV consumer that are within the 2 kV standard limits of the appliances. The more severe lightning levels (5 %) produced extremely high surge levels at the primary of the transformer. These high voltages would probably cause the network to fail however, before this occurs a high surge will be seen on the output of the transformer.

For the lightning simulations, as expected different loading configurations of the transformers did not yield a difference in the results.

Surges induced by the simulated operation of the feeder circuit breaker did produce any results of concern at the LV consumer level. Since these were not of a significant value surge arrestors are not necessary to protect for these types of switching surges. The various loading conditions also did not produce any results of interest.

The closing of the switch fuse disconnector at the Boyne View feed, as expected, showed that the loading of the Boyne View transformer affects the induced surges seen at the LV consumers. When the transformer was fully loaded surges of up to 10.7 kV are seen at the loads where as when it is lightly loaded this is reduced to less than 1 kV. It is for this reason that utility companies stress that electricity users turn off all non-essential appliances at the mains during a power outage to help protect against damage from these surges.

Chapter 8 Conclusion

8.1 Discussion

This thesis investigated the effects of power system disturbances on domestic appliances. A broad approach was taken to address the problem which included a study of power quality, identification of the standards applicable to power supplies contained within household appliances and the testing of the withstand limits of these supplies. In addition a model of a typical medium voltage distribution network was developed using the Power System Blockset in Matlab and a study was conducted into the level of transients that may be seen at the consumer low voltage terminal, in the event of lightning and switching surges occurring in the system.

The disturbance withstand experiments performed on the power supplies of domestic televisions/VCR's and personal computers, as described in Chapter 5, yielded little in regards actual damaging of the equipments. This result was expected since the tests focused mainly on checking that the power supplies were being manufactured accordingly with the required disturbance susceptibility standards. Initially the tests were to be performed to find the point at which the power supplies would fail; however this did not occur within the output range of the Schaffner Best EMC disturbance generator. It only offered an increase of 10 % above the standard limits, and this increase did not yield anything extra to the results. However, other studies, [1], have shown that the SMPS's of televisions and VCR's were damaged with surges between 4 and 6 kV.

The main issues identified from these experiments came from the voltage dip and transient burst testing. The LPX PC power supplies were affected by some voltage dip tests. The actual power supply components themselves were not affected but dips to 40 % for around 500 ms caused the power supply to shutdown and then restart when the voltage was restored. This resulted in a sudden reboot of the computer and loss of the data for the PC user.

The transient burst tests showed that the bursts were fast enough to travel through the power supply and onto its output resulting in a large increase in voltage on the output at these transient impulses. The tests did not affect the operation of the power supply and also did not affect the operation of a computer when they were applied to a functioning PC. It should be noted however that the surges were passing through the power supply into the appliance's sensitive circuitry. These internal components operate on a much lower voltage than the power supply input and can be highly sensitive to any interference on their voltage inputs, especially with the increasing complexity of microprocessors and motherboards etc. in personal computers. Although the tests conducted on the full PC did not cause any failures, in practice one would be concerned that the increased voltages would stress components causing degradation of performance and shortening their life considerably. This would also make them further susceptible to more energetic surges.

The results obtained from these tests are consistent with the finding of L.M. Anderson and K.B. Bowes [2]. From their testing of consumer electronic equipment (only clocks, microwave ovens and VCR's) they concluded that transients do not produce any adverse effects on the equipment but voltage dips resulted in loss of data and memory. S.B. Smith and R.B. Standler [1] found that when surges are applied to various electronic appliances, televisions and personal computer power supplies were the most vulnerable to upset and damage (Linear power supplies were not affected due to the large transformers used and their robust design). The surge voltage levels however that affected the televisions and PC power supplies were between 4 kV and 6 kV, higher than the permissible surge setting of the Best disturbance generator used here and higher than the limits set in the standards. The results obtained in the tests here corroborate the findings in this paper.

From the simulation of lightning on the MV distributor it was observed that the voltage and current levels experienced at the low voltage consumer loads varied depending on where the lightning surge was injected on the network. For the lightning injected at point 1 in Figure 7-15, the surge levels seen at the loads did not exceed the 2 kV surge withstand limit imposed by the EN 61000-4-5 standard for electrical appliances. For the other locations where lightning was injected the levels of surges experienced were much higher. The surge levels seen at the domestic appliances, however, depends on how

these surges are distributed throughout the loads connected, i.e. across the domestic dwellings fed from the phase conductor and the internal circuit branches within these residences. In all likelihood though, this would result in insulation failure and/or circuit breaker tripping on the network due to the extremely high voltages (over 1,500 kV) present and as a result the network feed would collapse, thus causing associated data loss problems in equipment without UPS protection.

Surge arrestors had the effect of limiting the voltage seen at the primary of the transformers thus limiting the level of surge seen on their output. Arrestors provide good protection for the network but are generally not installed as they can be costly and expensive to maintain and replace. They are installed however in areas experiencing high occurrence of surges through the network.

Switching surges at the start point of the network model did not yield surges of any significance at the consumer loads as they were dissipated through the distribution lines and transformers.

Switching surge simulations of a switch fuse re-closing at Boyne View estate did give some interesting results. When the consumer loads were lightly loaded and Boyne View network fuse connection was simulated the level of surge induced at this load only reached a high of 793.5 V. However, when the transformer was fully loaded the surge values reached was up at 10.7 kV and would certainly result in equipment damage. For this reason it is recommended that customers switch off all non essential appliances they can so there is little load present when the power is restored and thus reducing potential equipment damage from induced surges.

The results obtained show that lightning and switching on networks should be of major concern to utility companies. Lightning of course, cannot be controlled or prevented by man but there are ways to protect against its devastating effects. Switching surges are induced by activity on the network. This should be controlled and the effects along the network should be monitored.

8.2 Future Work and Recommendations

There are an infinite number of simulation configurations that could be performed on the network model. The ones most likely to present serious problems to utility companies are simulated and presented here.

Further work with regard to the analysis of the network model should incorporate obtaining statistical information from the ESB and building a database of actual measurements on the ESB network grid. A switching operation on the network should be setup and recordings obtained. These should then be analysed and compared with the simulation results obtained.

The model used here represents a section of network in a rural area. A more urban based setup should also be constructed and simulated using actual physical data obtained from the ESB.

At the time of writing, there is much heated debate amongst industry and equipment manufacturers regarding the introduction of the EN 50160 standard [49] (see accompanying workbook). This standard is currently a work in progress and is being pushed by utility companies to be brought into force. EN 50160 describes many supply voltage characteristics for electricity supplied by public distribution systems, such as voltage dips, transient overvoltages etc. It is claimed to present a realistic picture of the quality of electrical power as distributed today and specifies voltage surges and voltage variations levels which can be "expected." It is the general consensus by equipment manufacturers that the quoted values in the standard are very much in excess of those specified in the international product standards. For example, EN 50160 specifies voltage surge limits of 6 kV, whereas the standards pertaining to the power supplies discussed in this research specifies voltage surge limits of 2 kV. Therefore from this, all equipment manufacturers (of any product that receives electrical power from a utility company) will have to drastically redesign and test their equipment to ensure susceptibility to this new more severe surge limit. This would represent a significant extra cost which is sure to be passed on to, and which will be strongly contested by, the final user. The new proposal of the standard will also result in reduced mains power

quality which may lead to drastic increases in product damage and include possible safety concerns. Building's electrical infrastructure wiring and equipment will also need to be revised. From an equipment user and manufacturer perspective, it is felt that surge damage is not a significant problem today, therefore reducing the quality requirements of the supply will be seen to have serious consequences.

This is seen as an attempt to shift a lot of the burden of disturbance related problems from the utility companies to the equipment manufacturing industry. Many trade associations, such as the European Industry Association (EICTA) [50], Intelect [51] and Orgalime [52] are calling for the EN 50160 standard to be withdrawn or to be adapted (clearly saying that the standard does not apply to manufactured products such as appliances, portable tools and other household and similar loads) so it will not create the conflict with the current European standards.

The results presented in this thesis research have shown that for surges up to 2.2 kV, appliance power supplies are not affected but previous work carried out by S.B. Smith and R.B. Standler [1] has shown that appliances do experience malfunction and damage when subjected to surges between 4 kV and 6 kV. If this standard is to become mandatory in the future then it is clear that the new limits will result in equipment damage and that widespread redesign, with associated manufacture and cost implications, will be required. Presently designed appliances will not pass the EN 50160 standard limits.

The progress of this standard should be careful monitored as it will have vital impact on any future work in this area.

The research undertaken here has been broadly based, involving elements of testing according to international standards, simulation of power supplies and network analysis. A similar approach may be taken as a means of assessing the impact of any new standards in electronic equipment.

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- 52 Orgalime, http://www.orgalime.org/

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Appendix A: Additional Power Quality Information

A.1 Current drawn by a modern energy efficient lighting

To illustrate how a modern load operates compared to its traditional counterpart Figure A-1 shows current waveforms drawn by a modern energy efficient light and a standard older incandescent equivalent.

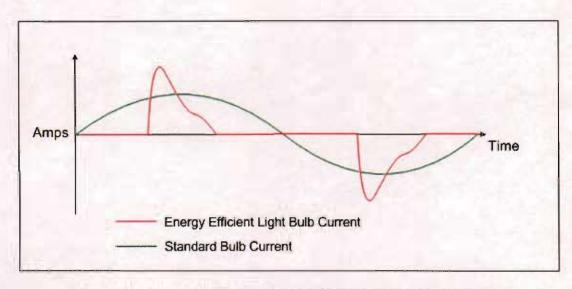


Figure A-1 - Current drawn by an energy efficient bulb vs. a standard bulb

The effective rms current drawn by the energy efficient bulb (EEB) is quarter that of the standard linear bulb. The EEB draws its current in pulses which leads to a distorted waveform when compared with the sinusoidal linear waveform of the standard bulb. Its efficiency is greater since it is not drawing current one hundred percent of the time. Many modern loads operate in this same non-linear manner, most common examples of which are switch-mode power supplies (found in most household appliances) and variable speed drives. The distortion introduced by these non-linear loads can cause problems on the electrical system and affect the operation of other equipment connected to the same supply.

A.2 Cost and effects of Power Quality

According to American based company Power Quality Inc.¹, the increasing use of sensitive electronic equipment is increasing the costs incurred by power disturbances. In 1970's typical costs were estimated at \$10 million, whereas in the 1980's this rose to \$100 million. And when these types of equipment really became commonplace in the 1990's the estimated costs relating to power disturbances are \$1 billion.

Studies carried out by the Electrical Power Research Institute (EPRI) show the losses to industries can be extremely high. Some of their findings include:²

Automotive Industry - \$50,000 to \$500,000 per event

Semiconductor Industry - \$350,000 per event & up

Chemical Industry - \$50,000 to \$500,000 per event

Equipment Manufacturers - \$100,000 per event

85 % of power quality problems, according to the EPRI, occur on the customer's side whilst the remaining 15 % may be attributed to lightning, wind, ice, snow, animals, utility equipment failures and switching of utility system equipment such as capacitors and reclosers.³ Solutions to correct these disturbances and/or to protect against them are highly recommended.

As can be seen, the consequences of poor power quality can be costly. Amongst others, poor power quality can cause electrical faults, fire hazards and threaten personnel safety.

Power quality is a large issue with industrial industries but is also a major concern for commercial and residential consumers. Highly sensitive equipment such as computers, fax machines, printers, photocopiers and televisions can be affected by disturbances, and can also contribute problems themselves in the form of harmonic distortion. Office

¹ Power Quality Inc., http://www.powerqualityinc.com

² Electrical Power Research Institute (EPRI), http://www.epri.com

³ Utilicorp, Power Quality Network, http://www.utilicorp.com

environments can contain a huge number of these types of loads which may present problems within the office building wiring. Neutral conductor runs and sizing considerations need to be assessed when the buildings are constructed.

Some problems are easily detected, whilst some, such as earthing faults and extremely short transients are more difficult to detect. For example, if the lights flicker and a PC reboots suddenly, a power quality voltage sag problem is most probably present. Likewise, if a television experiences interference caused by, say, a local sewage pump operating a variable speed drive nearby, a power quality problem is present.

In frequency of occurrence, power quality problems can be broken down as follows:4

- o User loads
- o User electrical system and grounding
- o Weather related i.e. lightning, wind, rain etc.
- Utility distribution
- Utility transmission
- Utility generation

A.3 Harmonic Distortion

Harmonic distortion problems have become more prevalent in the past decade with the increasing use of non-linear loads.

In an ideal electrical distribution system, power is at a constant voltage and frequency level. However in reality the voltage waveform can become badly distorted. This distortion is a result of *harmonics*.

Non-linear loads cause distortion by using electrical power at a different frequency than the 'fundamental' 50 Hz (60 Hz in the U.S.). Examples of such equipment would be television and radio receivers, computers (common PCs) - all of which use switch-mode

⁴ Chandler, T., "Power Quality: A World Wide Problem," Power Quality Inc.

power supplies, which are much more common today - and VSDs (Variable Speed Drives) etc.

In 1822, the French mathematician, Fourier, laid the basis for harmonic analysis. His basic concept was that any periodic function can be represented by the summation of a fundamental sinusoidal component with a series of higher order harmonic components having frequencies which are integer multiples of the fundamental frequency. This is known as the 'Fourier Series.'

Fourier analysis allows the distorted waveform to be broken down into a set of sine waves with certain frequency and magnitude characteristics. Waveforms that are not sinusoidal are said to be distorted and equivalent to adding one or more pure sinewaves at different frequencies, as illustrated in Figure A-2.

The distorted waveform repeats itself at the fundamental frequency, usually 50 Hz. Each successive sinewave, or harmonic, of this set has a frequency that is a multiple of the fundamental frequency. Hence, the 2nd harmonic has frequency 100 Hz, 3rd harmonic at 150 Hz, 4th at 200 Hz and so on.

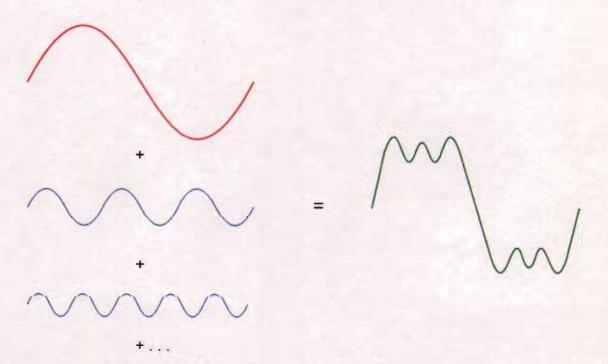


Figure A-2 - Addition of sinewaves leading to harmonic distortion

The magnitude characteristic, also called the *Harmonic Distortion Factor*, of each harmonic is represented as a percentage of the RMS value of the <u>fundamental</u>, not the total RMS of the distorted waveform. A harmonic analyser determines the magnitude.

The aggregate effect of all harmonics is called the 'Total Harmonic Distortion (THD)'

$$\%THD = \frac{\sum RMS \ of \ all \ Harmonics}{RMS \ of \ Fundamental} \times \frac{100}{1}$$

The "odd harmonics" (3rd, 5th, 7th, 9th, etc.) are symmetrical with respect to 90° whereas the "even harmonics" (2nd, 4th, 6th etc.) are asymmetrical with respect to 90°. What this means is, at 90°, the odd harmonics are at a positive or negative peak and even harmonics are at the zero crossing points.

In three phase power systems, the "even harmonics" (2nd, 4th, 6th, etc.) cancel, so we only need deal with the "odd harmonics."

The most common harmonics that stress networks are the 3rd, 5th and 7th harmonics with frequencies 150 Hz, 250 Hz and 350 Hz respectively. Generally, single-phase loads generate the 3rd harmonic and three-phase loads generate the other two. The 5th and 7th harmonics are easily filtered out by means of so called "tuned circuits" whilst, until recently, the 3rd's influence proved more difficult to filter out.

Harmonic No.	3	5	7	9	11	13	etc.
Phase	0	1	+	0		+	etc.
Sequence			40000		the state of		

Table A-1 - Sequence of the odd harmonics

The effects of the harmonics on the phase sequences are summarised as follows:

Sequence	<u>Direction</u>	<u>Effects</u>
+	forwards	Heating
	backwards	Heating and problems for motors
0	_	Heating and Accumulation in the
		Neutral Conductor

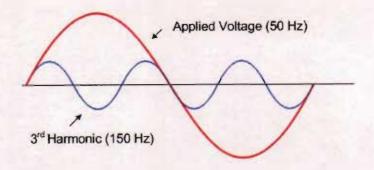


Figure A-3 - Third Harmonic waveform

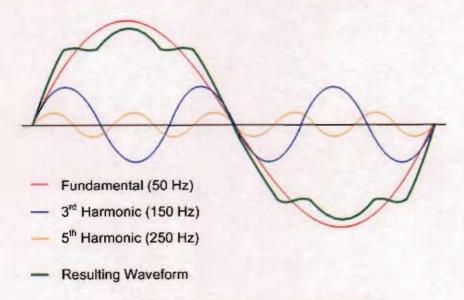


Figure A-4 - Addition of Odd Harmonics

Figure A-3 shows the fundamental and the 3rd harmonic. It is seen that there are three cycles of the third harmonic for each single cycle of the fundamental.

Figure A-4 shows the affect the addition of the fundamental 50 Hz sine wave and the 3rd and 5th odd harmonics has on the resulting waveshape. The result is a non-sinusoidal distorted waveform.

Triplen Harmonics are harmonics beginning with the 3rd and multiples of three after that. These are of particular importance and cause the most problems on the electricity system. If there are balanced 50 Hz currents on all three phase conductors, the neutral current will add to zero. The 3rd harmonic of each of the three phase conductors is exactly in phase. When these zero-sequence triplen harmonic currents come together on

the neutral, rather than cancel, they actually add up resulting in there being more current on the neutral conductor than on the phase conductors. This problem is particularly prevalent with single-phase electronics based loads.

In Figure A-5 the 3rd harmonic is at the same stage in each phase of a three-phase system, causing the current generated by the harmonics to accumulate in the neutral conductor.

There can be a risk of fire because the neutral conductor is not protected by a fuse. The neutral conductor may need to be 'oversized' at the design stage.

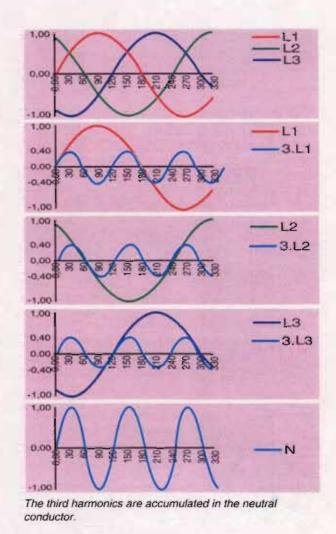


Figure A-5 - Third Harmonic in the neutral conductor⁵

According to the international EMC directive regulations regarding the dimensioning of the neutral conductor and taking into account the load in the neutral conductor caused by third harmonics, the cross-section of neutral conductors must be the same as the cross-section of the phase conductors in single-phase circuits whilst in polyphase circuits it is only necessary up to 16mm² copper or 25mm² aluminium.⁵

Examples of such equipment that generate triplen harmonics are:5

- Computers
- Office equipment
- Welding equipment
- Generators

- Rectifiers
- UPS
- Home electronic appliances

There are numerous ways of reducing harmonic content, such as series and shunt filtering (the shunt being the preferred) and Zig-Zag transformers.

Computers and electronic equipment used in residential and commercial/office environments usually employ filtering at the power supply input to eliminate the effects of noise and voltage transients. If these were to pass through the power supply into the equipments sensitive circuitry it could result in damage and/or data corruption and malfunction. Metal Oxide Varistors (MOVs) are usually used to help protect the appliance from transients. They are also effective for high frequency noise but do not prevent the power supply from drawing large current pulses and introducing harmonics to the supply system.

Power factor correction can also be incorporated into the design of these types of equipment to help limit the harmonics injected back into the system.

The third harmonics that accumulates in the neutral in three-phase industrial systems has long been a problem as well as being difficult to come up with a solution. This however cannot be completely solved but there are costly products that can come close to fully eliminating the harmonics.

Third Harmonic Filters (THFs) can be used to eliminate these 3rd harmonic problems. One such THF developed by ABB Control⁶ eliminates about 95 % of the 150 Hz current in the neutral conductor. It forms a high resistance at 150 Hz, obtained by trimming an inductor and capacitance, coupled in parallel to **the load, to resonate** at the required 150 Hz frequency. It also eliminates the 150 Hz current in the phase conductors. Its benefits

⁵ ABB Control, "Enclosed Third Harmonic Filter THF Solutions," Technical Brochure THF 1 GB 99-03

⁶ ABB Control, "Third Harmonic Filter THF," Technical Brochure THF 1 GB 96-11/97-11

include increasing the life of capacitors and considerably decreasing maintenance costs. Also the risk of fire and the operating temperature of transformers both decrease as well as magnetic fields and power consumption. Overall, it improves power quality.⁵

If the value of the 150 Hz component exceeds 15 % of the phase current, a THF is usually recommended.

Installation of the THF requires careful assessment. The standard earthing method used in industry in Ireland today is the TN-S (as shown in Figure A-6), (T=Terrain, N=Neutral, S=Separate Earth & Neutral Conductors). The method used for residential consumers is TN-C-S (C=Combined Earth & Neutral on the same conductor). In industrial facilities, it is advisable to install the THF in the transformer star point (neutral) to ensure the THF cannot be bypassed beyond on the load side (a spurious N-E connection). Therefore no third harmonic (150 Hz) voltage exists between the neutral and the earth (PE). As these third harmonics appear on the neutral, placing the THF in this fashion effectively eliminates harmonic currents on the neutral.

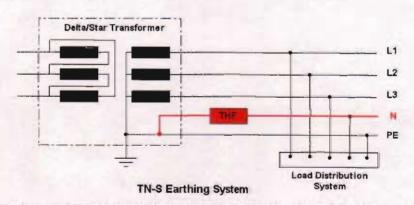


Figure A-6 - Third Harmonic Filter installation in a TN-S earthing system

A.4 Additional disturbances information

Earthing is another important issue for power quality since it is part of a safety system to protect personnel and equipment. Zero volts and no current or noise needs to be maintained on the earthing system, as it acts as a reference for most electronic

equipment. IEEE Standard P1100⁷: Guide for Powering and Grounding Sensitive Equipment outlines the guideline standards for such equipment.⁸

Other power system disturbances resulting in decreased power quality include:

- Flicker
- Electromagnetic Interference/Noise (EMI)
- Radio Frequency Interference (RFI)
- · Bad Wiring

- Interharmonics (distortion)
- Voltage Imbalance
- Notching (distortion)
- Power Frequency Variations

Flicker, as mentioned previously, is a phenomenon related to voltage fluctuations and associated with lighting systems. It is usually an observed disturbance where the observer will notice the light source "flickering." This can be annoying, sometimes causing headaches and is especially dangerous for people suffering from epilepsy. The flickering effect can in severe cases trigger a seizure. The European standard relating to flicker is EN 61000-3-3:2001 Limitation of voltage fluctuations and flicker in low-voltage supply systems for equipment with a rated current < 16A⁹.

Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) may be conducted or radiated. The radiated noise travels through the air and can interference with communications and sensitive electronic equipment. Harmonics usually increase the likeliness of both. Incorporating proper shielding will help reduce their effects.

Interharmonics are similar to harmonics but are voltages or currents having frequency components that are <u>not</u> integer multiples of the supply frequency. The main sources of interharmonic waveform distortion are static frequency converters, cyclo-converters,

ANSI/IEEE Standard 1100: The Emerald Book, IEEE Recommend Practice for Powering and Grounding Sensitive Electronic Equipment

⁸ Utilicorp, Power Quality Network, http://www.utilicorp.com

⁹ EN 61000-3-3:2001 Limitation of voltage fluctuations and flicker in low-voltage supply systems for equipment with a rated current <16A</p>

induction motors and arcing devices. The effects of interharmonics are not well known. They have been shown to affect power line carrier signalling, and induce visual flicker in display devices such as cathode ray tube (CRT) monitors.

Notching is a periodic voltage disturbance caused by the normal operation of power electronics devices when current is commutated from one phase to another. When the current commutates from one phase to another there is a momentary short circuit between two phases pulling the voltage as close to zero as permitted by system impedances.

A.5 Loads affecting Power Quality

As explained previously the introduction of non-linear loads, power electronics and sensitive equipment have resulted in a greater need for a higher quality electricity supply. They have introduced distortion into the electricity supply system and have also become more susceptible to variations in the supply. As mentioned before typical non-linear loads are equipment incorporating switch-mode power supplies, variable speed motor drives and silicon controlled rectified (SCR) loads.

Switch-mode power supplies (covered in greater detail in chapter 4) are used to provide a constant voltage to an appliance. The current drawn by these power supplies is non-sinusoidal and introduces noise to the power system. Its basic operation is to convert the a.c. input into a constant d.c. output. The a.c. is rectified to d.c. which is then smoothed by filtering capacitors. A transistor device acts as a high frequency switch to provide d.c. pulses that are smoothed to give a constant d.c. by an output filter. This switching action results in the power supply injecting harmonics into the supply system. Current is drawn from the supplies only at the peaks of the voltage waveforms and this pulsating current leads to a flattening of the voltage waveform. As well as having uses in residential appliances switch-mode power supplies are found in nearly all office

¹⁰ Electrotek Concepts, http://www.electrotek.com

equipment and are used in fluorescent lighting applications, which make up in the region of 50 % of modern buildings loads. Modern commercial buildings have had to install large neutral conductors to cope with the levels of third harmonics presented from these types of equipment. The issue of harmonic problems in modern buildings is covered in an article entitled "Power monitoring and harmonic problems in the modern building" by Eugene Conroy¹¹.

Variable speed drives (VSDs) operate on the same principles but are inverters. These are however used on three-phase systems. VSDs are wired as three-phase loads and therefore do not produce triplen harmonics. They can be therefore used for approximately 30 - 50 % of a facility's load but if there is power factor correction capacitors present at the facility or if the 50 % load is exceeded it is advised to install harmonic filters. They are however highly susceptible to voltage dip disturbances and cause problems in processes where loss of mechanical synchronisation is an issue.

Silicon Controlled Rectified (SCR) loads only conduct for part of each half cycle. Repetitive abrupt current impulses on each half cycle are the result of this operation and this introduces significant noise. These impulses may exceed the energy ratings of the devices and can also present timing related problems. Good filtering is required to prevent damage.

Convoy E., "Power monitoring and harmonic problems in the modern building," *IEEE Power Engineering Journal*, vol. 15, pp. 101-107, April 2001

¹² Kernan, D., "Power Quality Methods and Techniques," PEI Technologies

A.6 Power disturbance protection techniques

There are numerous devices available to help the electricity consumer achieve constant 'clean' power and to protect against disturbances. If a reactive approach is taken to the problems then a full understanding of their nature needs to be first realised. Generally a proactive approach is advisable, especially in industrial facilities. It can be costly but when compared to the costs associated with power disturbances it is considered a worthwhile investment.

Devices such as Transient Voltage Surge Suppressors (TVSS) - which absorb extra energy above a certain level before reaching the load - line tracking filters, isolation transformers and active power factor correction circuits can be used to prevent disturbances related problems in industrial environments.

In residential situations there are two major ways to protect equipment. The first involves protection installed at the point of entry, at the electrical panel/meter and the second involves installation at the point of use i.e. the electrical output sockets. A combination of these will provide the best protection.

At the entry point panel surge-suppression devices can be attached to the meter. They provide the first line of defence against surges into the house from the power lines. The utility company can only install these. Another method involves the installation of protection surge-suppressors in panel board branches. This helps to prevent surges that originate on one of the house's electrical circuits from spreading to other circuits.

Devices for use at the point of equipment include *plug-in surge suppressors* and 'Uninterruptible Power Supplies' (UPS). Plug-in surge suppressors are usually designed into some power strips extension blocks and can also include jacks for data communication protection too. They are affordable but have somewhat limited protection for sensitive equipment and as with everything the more the consumer pays the better protection they will receive.

Home computer UPS's are installed as in-line devices. There are various different UPS types depending on the installation conditions. An in-line device in place between the wall outlet socket and the appliances input. During normal operation the UPS takes the

a.c. input and provides filtered a.c. on its outputs. When a voltage drop or power failure occurs the UPS isolates the input a.c from its outputs and a d.c./a.c. inverter provides a step wave a.c. output of 230 Vrms (or 115 Vrms in the U.S.) A lead acid battery is used as the inverter power source. The end user will therefore experience no break in the input supply. If there is a power failure however the battery capacity is utilised. And of course the more one pays the greater the capacity of the included battery. The battery can usually supply the appliance with full a.c. voltage for anything between 4 minutes and 15 minutes. After which the appliance will shut down if the power is not restored. UPS's are essentially used to protect the data that the user may be working on at that the moment of the disturbance. It allows time to save the work being carried out and to shutdown the computer safely until the power has been restored. After which the UPS battery will be recharged. More expensive UPS's work in an on-line state as opposed to off-line as described above. Here the UPS is not bypassed and it provides a sine wave on its output to continuously run the loads and recharges the battery system at the same time.

Appendix B: History and Development of Power Supplies

As the electronics industry began to boom in the early 1960's, the main emphasis was on miniaturisation. Developing smaller and more power efficient equipment was a key aim of designers of electronic equipment. The introduction of the transistor and the development of integrated circuits in the previous decade paved the way forward for this thinking. In order to achieve this, the equipment's power supplies also had to develop towards miniaturisation and greater efficiency.

The electronic equipment being developed required a low operating voltage and most often a d.c. source too. A local power supply was needed to convert the mains a.c. to d.c. A power supply (sometimes referred to as a power converter) is essentially a buffer circuit that is placed between the mains incompatible source and a load in order to make them compatible. The Power Sources Manufacturers Association's (PSMA) Handbook of Standardised Terminology for the Power Sources Industry gives the definition of a power supply.

Power Supply – a device for the conversion of available power of one set of characteristics to another set of characteristics to meet specified requirements. Typical application of power supplies include raw input power to a controlled or stabilised voltage and/or current for the operation of electronic equipment¹³.

Switch-mode power supplies had been commonplace in military and avionic equipment long before they found their way into consumer electronics. Until the 1970's or so, most consumer electronic equipment used a basic power transformer/rectifier/filter capacitor type power supply.

A typical mains connected power supply must perform the following functions:

- Voltage Conversion changing the mains voltage to a level determined by application
- Rectification converting a.c. into d.c.
- Filtering to smooth ripple on the rectified voltage

¹³ Foutz, J., http://www.smpstech.com

- Regulation ensuring the output voltage(s) is independent of mains and load variations
- Isolation separating the outputs from direct connections to the a.c. mains

Linear power supplies (as shown in Figure B-1) were traditionally used. These fixed voltage regulated power supplies maintained a constant output voltage by using a transistor, or a special IC, as a series resistor whose value of resistance is controlled so as to maintain the output voltage constant despite variations in load. The equivalent circuit of a series regulator is shown in Figure B-2. It works well but is highly inefficient as a lot of power is dissipated as heat. Linear regulation is mainly used in low power applications where some lost heat is not a problem (in higher power applications switched more power supplies are preferred because of less wasted power and greater efficiency).

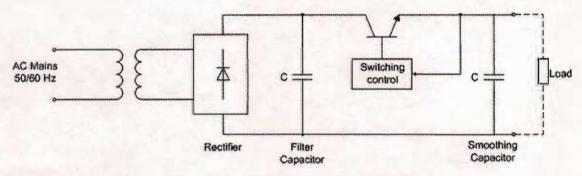


Figure B-1 - Linear Power Supply Schematic

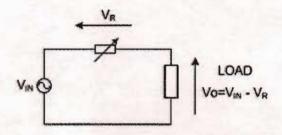


Figure B-2 - Linear Series Regulator Equivalent Circuit

A linear power supply can only step-down an input voltage to produce a lower output voltage. The transistor is operated in its linear mode. Operating in this mode means that there is always a headroom voltage between the input and the output. As a result, the regulator dissipates a considerable amount of power. This headroom voltage loss causes the linear regulator to be 35 to 65 percent efficient. A large heatsink is required to dissipate the heat generated by the regulator and very large filter capacitors are required

to store enough energy to maintain the output for a reasonable length of time if the mains voltage is somehow removed. The low frequency mains transformer is also heavy and bulky and the cost of the heatsink and the transformer makes linear power supplies generally uneconomical for applications above 10 Watts. They are however used in most audio equipment due to noise issues when using the switch-mode variety.

Appendix C: Personal Computer Power Supplies

C.1 DC Output Voltages

The input into the power supply is usually user selectable between 115 Vac and 230 Vac depending on where in the world the computer will be used. The power supply outputs multiple d.c. voltage levels, positive and some negative. *Note:* there have been various standard PC power supply models. They vary by the physical dimensions of the power supply chassis and also the output connectors and output voltage values. These are discussed further later in this section.

The typical output voltages supplied to the computer are:

- + 3.3 V (introduced in ATX power supplies see later)
- +5 V
- + 12 V

The 3.3 V and 5 V outputs are used by digital circuits. Typically, on older systems, the + 5 V line was used to run the motherboard, the CPU and almost all other components of the computer system. When Intel introduced the second generation Pentium microprocessor chips they reduced its voltage to 3.3 V in order to reduce power consumption as the chips got faster and the tracks got even closer. The ATX form factor power supply was introduced and provided the +3.3 V directly. New CPUs, some types of system memory and graphics cards use the +3.3 V line while the motherboard and other components still use +5 V. The +12 V and +5 V outputs are used to power disk drives and fans. An internal connection off the +12 V output powers the power supplies fan.

Computer power supplies also have -12 V and -5 V outputs. They are not used much nowadays but are included to provide compatibility with older hardware; the -12 V was used for serial port circuits and the -5 V used by ISA bus cards.

C.2 Power Supply Form Factors

The term form factor describes a computer system's design in terms of general shape and dimensions and connections. Power supplies have to be built to accommodate these

form factor specifications in order to fit into the pc chassis and connect correctly to the motherboard it is to provide power to.¹⁴

Summaries the different computer form factor designs from the first one, PC/XT, to the ones used today.

Form Factor	Dimensions (w x h x d)	Style	Motherboard Connector	Output Voltages
PC/XT	222 x 120 x 142	Desktop	AT Style	+/- 12 V, gnd +/- 5V
AT	213 x 150 x 150	Desktop or Tower	AT Style	+/- 12 V, gnd +/- 5V
Baby AT	160 x 150 x 150	Desktop or Tower	AT Style	+/- 12 V, gnd +/- 5V
LPX	150 x 86 x 140	Desktop	AT Style	+/- 12 V, gnd +/- 5V
ATX/NLX	150 x 86 x 140	Desktop or Tower	ATX Style	+/- 12 V, gnd +/- 5V, +5V _{SB} + 3.3 V
SFX	100 x 63.5 x 125	Desktop or Tower	ATX Style	+/- 12 V, gnd + 5V, +5V _{SB} + 3.3 V-V _{Sense}
WTX	150 x 86 x 230 (single fan) 244 x 86 x 230 (double fan)	Tower	WTX Style	+/- 12 V, gnd +5V, +5V _{SB} +3.3V, +3.3/5V _{Sense}

Table C-1 - Personal Computer Form Factors

The PC/XT form factor was the first developed by IBM, who invented the modern personal computer. Initially they had a low power rating of 63.5 W and when hard disk drives were introduced this doubled to 130 W. Its successors the AT and Baby AT form factors were introduced by IBM in 1984 and started the boom in the PC world. They were the first "tower" style PCs. The output power was boosted to 192 W and they included remote power switches at the front of the PC. The smaller Baby AT design was most popular from 1985 until 1995.

¹⁴ The PC Guide, http://www.pcguide.com

In the late 1990's the *LPX form factor* specification replaces these and introduced a significant size reduction which aided design of much smaller PCs.

The diagram in Figure C-1 shows the dimensions of the LPX power supply.

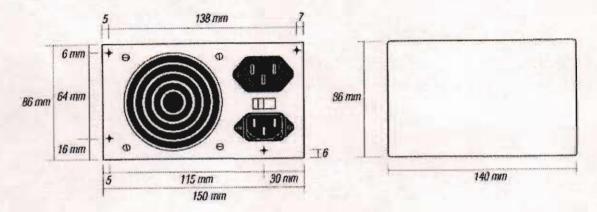


Figure C-1 - LPX Form Factor Power Supply Dimensions - side and rear view

(source: PCGuide.com)

The LPX power supplies were the type available in personal computers around the time the utility company sponsor of this work experienced the increase in damage claims, as indicated in an internal email discussion within the utility company a number of years back. Some of this type of power supply was used in the EMC immunity tests (see chapter 5).

The LPX power supplies were produced in large quantities and millions of these power supplies are still in use today.

The most significant change in computer design since the invention of the PC came when Intel introduced the ATX form factor in 1995. After several years before this form factor caught on, it is now standard in the majority of the marketplace. In order to avoid other form factors emerging, Intel created the ATX/NLX motherboard and PC chassis to use its new ATX power supply. The internal design of the ATX power supply had changed significantly over the LPX form and the output connectors also changed therefore requiring new a new motherboard and computer chassis. This of course meant that the ATX format was not backwards compatible as was the case with the previous form factors that came before it.

On the outside the ATX power supply has the same dimensions as its LPX predecessor but the monitor pass-through connector is removed since modern monitors come with their own power supply units.

As mentioned before, ATX power supplies were the first to include the +3.3 V output directly. It also introduced additional signal outputs for use by the motherboard and for fan control. These are discussed further later in this chapter.

The SFX/microATX form factor is part of the trend towards smaller PCs. The dimensions are smaller to that of the ATX and as such the power output is around 90 W which is sufficient to run small systems with low-powered CPUs and few peripherals but leaves little room for expansion. Its motherboard connector is the same shape and size of the ATX connector. The 20 pin connector has nineteen same connectors as the ATX one. A 'Fan On/Off' signal (for thermal speed control) places the -5 V voltage pin. The SFX power supply specification does not include the -5 V line. This is because the -5 V is only required for ISA bus compatibility and since this had become redundant Intel chose to move forward towards new systems and intentionally left the -5 V line out.

ATX and microATX power supplies were also EMC immunity tested and this is covered further in chapter 5.

The WTX form factor, introduced again by Intel in 1998, is designed specifically for workstations. It is totally different than the other PC form factors as it is designed to meet the needs of larger systems which can include multiple microprocessors.

C.3 PC Power Supply Output Connectors

Drive power connectors

Power supply drive power connectors are shown in Figure C-2.

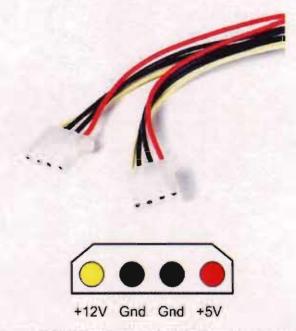


Figure C-2 - PC power supply drive power connectors

The power supply provides power to internal hard disks and removable media such as CD/DVD/CD-RW/DVD±RW drives and zip drives through the connector shown. The connector has a +12 V and +5 V lines and two ground return paths.

Motherboard power connectors

This is the most important connector in the computer system. The two connector configurations shown in Figure C-3 were traditionally used in PC/XT, AT, Baby AT, and LPX form factors and is now referred to as an 'AT style' connectors. The recent ATX style connector is shown in Figure C-4.

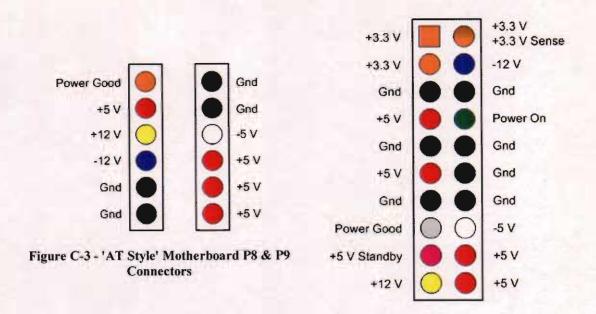


Figure C-4 – 'ATX Style' Motherboard Connector

The "power good" signal (nominally about +5 V) is basically a safety signal for the motherboard. When someone starts a PC from cold the power supply may take some time (typically half a second or more) to generate the required d.c. output voltages and stabilise. When this is complete the power supply sends a signal on the power good line to the motherboard telling it that the power supply is ready for use. If the motherboard allowed the computer to boot up right from the start it could result in data errors and corruption if the correct voltages were not present. The power good signal is used to prevent this.

If the power supply malfunctioned in any way e.g. if it is hit by a surge or experiences a reduced or completely dropped voltage, it will turn off the power good signal. When the power is ok again is turns the signal back on. This type of occurrence will reset the computer and cause it to suddenly, without warning, reboot itself.

The ATX style single piece connector uses twenty pins with a square hole for pin one to ensure correct connection.

The 'Power On' and ± 5 V standby signals at are used for what is known as "Soft Power." The form factors that came before ATX used a mechanical switch to turn the computer on and off. From the ATX form factor onwards this switch was replaced by a signal from the motherboard telling the power supply what to do to. The motherboard

can also be told to change this signal by software control thus allowing Microsoft Windows to shut down the PC and turn it off. The 'power on' signal controls the power supply in this manner. In order for the motherboard to be able to tell the power supply to turn on the motherboard needs to have power available all the time. The +5 V standby line is always on, even when the rest of the power supply is turned off, and a small amount of current on this wire is what allows the mother board to control the power supply when it is off. It also allows for other means of starting the PC such as modem or network activity activation.

In order to protect the microprocessor the +3.3 V Sense is used to detect the voltage level of the +3.3 V signal to the motherboard. This therefore allows the power supply to "fine tune" the +3.3 V output in the event of excessive voltage drop between the supply and the components that use +3.3 V.

As described previously SFX/microATX power supplies do away with the -5 V ISA compatibility signal on its motherboard connector.

Additional connections

An ATX power supply also features an auxiliary 1x6 connector and an optional 2x3 connector. These are used for motherboards that will require a lot of power to run their components (250 W or more)

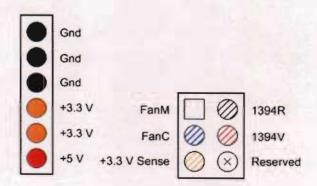


Figure C-5 - ATX auxiliary (left) and optional (right) connectors

FanC (Fan Control) and FanM (Fan Monitor) signals controls the speed of the power supply fan. The speed is proportional to the voltage on FanC.

In a SFX power supply the Fan ON/Off signal replaces the FanC signal.

1394R and 1394V signals provides a separate voltage circuit for powering IEEE-1394, or "Firewire," peripherals and is not used by the motherboard.

The WTX connectors will not be described further as they are not relevant to the work of this thesis.

C.4 Power Supply Certifications

All power supplies have their safety and quality certified by one or more agencies. They indicate that the power supply has been tested and passed certain standard directives.

The most common certification organisations acronyms or approval marks are UL (Underwriters Laboratories Inc.) in the USA, CSA (Canadian Standards Association) for Canada and the CE mark for products to be sold in the European Union.

Additional EMI/RFI compliance certifications from the Federal Communications Commission (FCC) (usually class B certification) may be included on products.

Energy Star compliance certification is also used to promote energy efficient PCs and components.

Appendix D: Power Supplies Tested: Specifications

The follow table gives detailed specifications of the LPX and ATX power supplies tested:

ATX 1:	Astec ATX	(90-3405 (micro	CE marked		
	Maximum C	Output Power: 90			
	Input:	100 – 127 V	/ac	~ 3 A max.	50 / 60 Hz
		200 - 240 V	/ac	~ 1.5 A max.	
	Output:	+ 12 V	1.5 A max.	- 12 V	0.2 A max.
	1	+ 5 V	12 A max.	- 5 V Standby	0.72 A max.
		+ 3.3 V	6 A max.		

ATX 2:	Sunny Tech	nologies Co. Ltd	. ATX-235C		CE marked
	Maximum C	Output Power: 23	5 Watts	AND ACT	
	Input:	115 Vac		~ 6 A max.	50 / 60 Hz
		230 Vac		\sim 3 A max.	
	Output:	+ 12 V	8 A max.	- 5V	0.5 A max.
	1	+ 5 V	22 A max.	- 12 V	1 A max.
		+ 3.3 V	14 A max.	+ 5 V Standby	1.5 A max.

LPX 1:	Astec SA1	45-3430			
	Maximum C				
	Input:	100 – 120 Vac 200 – 240 Vac		~ 6 A max. 50 / 60 Hz ~ 4 A max.	
	Output:	+ 12 V + 5 V	4.2 A max. 18 A max.	- 5 V - 12 V	0.3 A max. 0.3 A max.

LPX 2:	Siemens Nixdorf S26113-E354-V10						
	Maximum C						
	Input:	100 – 125 V 200 – 240 V			50 / 60 Hz		
	Output:	+ 12 V + 5 V	4.2 A max. 18 A max.	- 5 V -12 V + 5 V Aux	0.4 A max. 0.3 A max. 0.02A max.		

LPX 1:	Astec SA1	45-3430				
	Maximum Output Power: 145 Watts					
	Input:	100 – 120 Vac 200 – 240 Vac		~ 6 A max. 50 / 60 I ~ 4 A max.		
	Output:	+ 12 V		- 5 V - 12 V	0.3 A max. 0.3 A max.	

Dell PC	Dell PC Po	wer Supply						
	Input:	100 – 120 V 200 – 240 V		~ 6 A max. ~ 4 A max.	50 / 60 Hz			
	Output:	+ 12 V + 5 V	4.2 A max. 18 A max.	- 5 V - 12 V	0.3 A max. 0.3 A max.			

Appendix E: Sample Harmonic Measurement Test Results

E.1 Test results for ATX form factor switch-mode power supplies

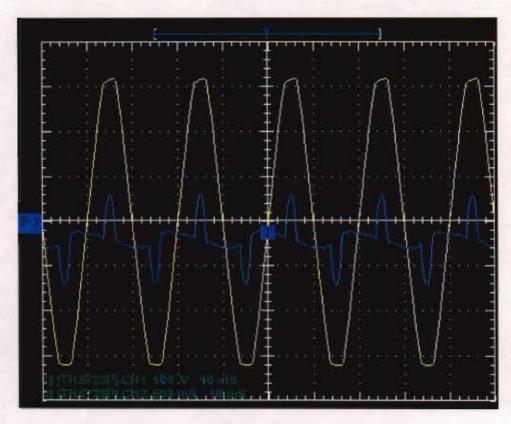


Figure 6 - ATX power supply voltage and current waveforms

The full test results obtained are:

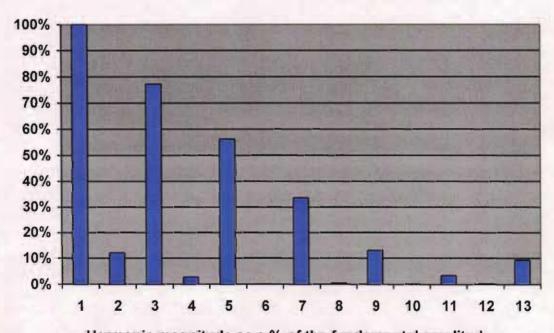
Voltage THD = 2.836 % Current THD = 103.239 %

Power Factor = 0.445 Displacement PF = -24.727

Apparent Power = 68.069 VA Reactive Power = 60.953 VAR

Harm No.	Freq.	Voltage RMS	Voltage % of Fund.	Voltage Phase	Current RMS	Current % of Fund.	Current Phase
Fund.	49.982 Hz	232.89 V	100.00%	0.0000	142.94mA	100.00%	0.0000
2 nd	99.965 Hz	1.8124 V	0.778 %	161.47	17.307mA	12.108 %	-169.72
3 rd	149.95 Hz	1.9726 V	0.847 %	73.896	110.24mA	77.126 %	48.061
4 th	199.93 Hz	331.17mV	0.142 %	6.4602	4.0849mA	2.858 %	93.033
5 th	249.91 Hz	5.1511 V	2.212 %	1.5718	80.332mA	56.200 %	-78.695
6 th	299.89 Hz	60.354mV	0.026 %	-76.357	195.58uA	0.137 %	-122.88
7 th	349.88 Hz	2.7884 V	1.197 %	173.75	48.014mA	33.591 %	151.29
8 th	399.86 Hz	58.947mV	0.025 %	-143.90	622.90uA	0.436 %	106.39
9 th	449.84 Hz	1.2257 V	0.526 %	-8.2109	18.659mA	13.054 %	27.679
10 th	499.82 Hz	10.997mV	0.005 %	81.234	129.53uA	0.091 %	24.851
11 th	549.81 Hz	388.57mV	0.167 %	-148.28	4.8123mA	3.367 %	16.598
12 th	599.79 Hz	113.45mV	0.049 %	125.13	423.80uA	0.296 %	492.51m
13 th	649.77 Hz	573.29mV	0.246 %	127.17	13.268mA	9.283 %	-74.793





Harmonic magnitude as a % of the fundamental amplitude

Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th
Standard Limit [mA]	103.020	57.57	30.30	15.150	10.605	8.973
Recorded Level [mA]	110.24	80.332	48.014	18.659	4.8123	13.268

E.2 Test results for LPX form factor switch-mode power supplies

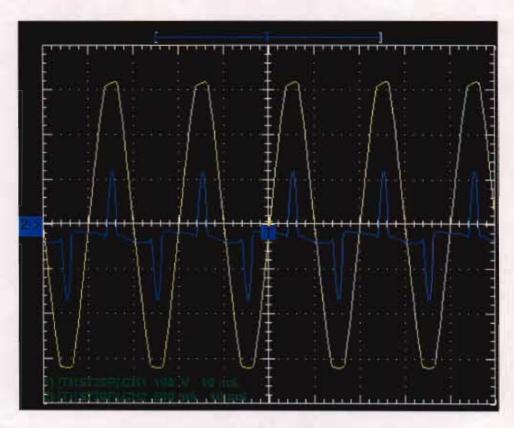


Figure 7 - LPX power supply voltage and current waveforms

The full test results obtained are:

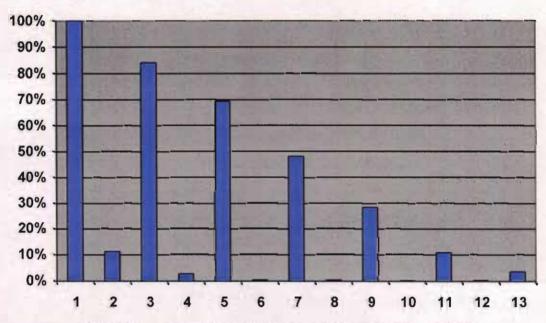
Voltage THD = 2.894 % Current THD = 123.638 %

Power Factor = 0.541 Displacement PF= -9.6703

Apparent Power = 67.348VA Reactive Power = 56.656 VAR

Harm No.	Freq.	Voltage RMS	Voltage % of Fund.	Voltage Phase	Current RMS	Current % of Fund.	Current Phase
Fund.	49.998 Hz	232.99 V	100.00 %	0.0000	159.65mA	100.00 %	0.0000
2 nd	99.997 Hz	1.8851 V	0.809 %	162.19	18.012mA	11.282 %	172.51
3 rd	149.99 Hz	2.1366 V	0.917 %	72.324	134.13mA	84.014 %	29.801
4 th	199.99 Hz	293.96mV	0.126 %	10.200	4.4065mA	2.760 %	39.755
5 th	249.99 Hz	5.2649 V	2.260 %	1.3151	110.89mA	69.459 %	-121.94
6 th	299.99 Hz	54.805mV	0.024 %	-70.348	725.24uA	0.454 %	158.34
7 th	349.99 Hz	2.6963 V	1.157 %	176.23	76.995mA	48.227 %	85.302
8 th	399.99 Hz	96.849mV	0.042 %	-134.68	763.32uA	0.478 %	10.051
9 th	449.98 Hz	1.2892 V	0.553 %	-6.6270	45.440mA	28.462 %	-65.676
10 th	499.98 Hz	13.122mV	0.006 %	-78.792	461.16uA	0.289 %	-64.069
11 th	549.98 Hz	435.52mV	0.187 %	-155.00	17.344mA	10.863 %	153.63
12 th	599.98 Hz	107.98mV	0.046 %	118.09	640.24uA	0.401 %	-152.07
13 th	649.98 Hz	620.52mV	0.266 %	121.46	5.9423mA	3.722 %	95.426





Harmonic magnitude as a % of the fundamental amplitude

Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th
Standard Limit [mA]	123.801	69.183	36.412	18.206	12.744	10.784
Recorded Level [mA]	134.13	110.89	76.995	45.440	17.344	5.9423

E.3 Test results for fully operating Dell Personal Computer

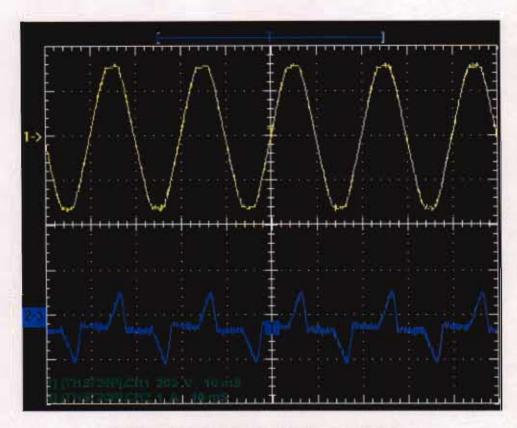


Figure 8 - Dell PC voltage and current waveforms

The full results obtained are:

Voltage = 232.75 V Current = 508.93 mA True Power = 57.529 W

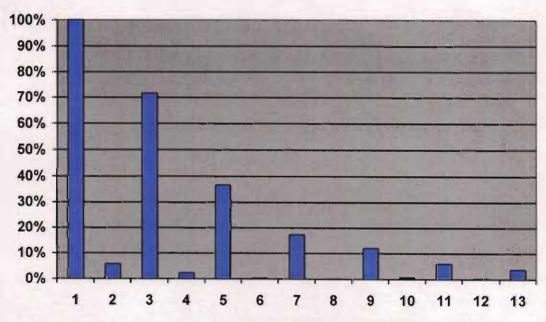
Voltage THD = 3.078 % Current THD = 83.621 %

Power Factor = 0.486 Displacement PF = 9.9122

Apparent Power = 118.45 VA Reactive Power = 103.55 VAR

Harm No.	Freq.	Voltage RMS	Voltage % of Fund.	Voltage Phase	Current RMS	Current % of Fund.	Current Phase
Fund.	50.025 Hz	232.37 V	100.00 %	0.0000	243.78mA	100.00 %	0.0000
2 nd	100.05 Hz	1.9302 V	0.831 %	165.28	13.947mA	5.721 %	172.38
3 rd	150.08 Hz	1.6789 V	0.723 %	86.706	174.56mA	71.606 %	40.114
4 th	200.10 Hz	871.35mV	0.375 %	94.809	5.7492mA	2.358 %	33.620
5 th	250.13 Hz	6.0964 V	2.624 %	-5.6450	89.010mA	36.513 %	-105.60
6 th	300.15 Hz	646.37mV	0.278 %	93.254	824.95uA	0.338 %	-107.82
7 th	350.18 Hz	2.1552 V	0.927 %	-175.74	42.184mA	17.304 %	144.30
8 th	400.20 Hz	227.31mV	0.098 %	-150.21	367.97uA	0.151 %	65.405
9 th	450.23 Hz	1.0553 V	0.454 %	-8.6354	29.141mA	11.954 %	25.166
10 th	500.25 Hz	504.69mV	0.217 %	-70.242	1.8903mA	0.775 %	106.10
11 th	550.28 Hz	168.13mV	0.072 %	-110.78	14.692mA	6.027 %	-91.841
12 th	600.30 Hz	75.881mV	0.033 %	-33.752	581.89uA	0.239 %	-175.36
13 th	650.33 Hz	280.87mV	0.121 %	77.473	9.0974mA	3.732 %	-175.94





Harmonic magnitude as a % of the fundamental amplitude

Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th
Standard Limit [mA]	195.599	109.31	57.529	28.7645	20.135	17.037
Recorded Level [mA]	174.56	89.01	42.184	29.141	14.692	9.0974

E.4 Test results for Dell Personal Computer operating in standby

Voltage = 225.3 V Current = 170.6 mA

True Power = 3.299 W

Voltage THD = 2.9 %

Current THD = 96.8 %

Power Factor = 0.08

Displacement PF = 0.40

Apparent Power = 39.05 VA

Reactive Power = 38.96 VAR

Current Odd Harmonics	% fundamental	[mA]
Fundamental	100 %	33.68 mA
3 rd Harmonic	40.4 %	13.61 mA
5 th Harmonic	44.9 %	14.97 mA
7 th Harmonic	28.9 %	9.706 mA
9 th Harmonic	15.9 %	5.338 mA
11 th Harmonic	9.6 %	3.157 mA
13 th Harmonic	8.5 %	2.796 mA

Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th
Standard Limit [mA]	11.217	6.268	3.299	1.650	1.155	0.977
Recorded Level [mA]	13.61	14.97	9.706	5.338	3.157	2.796

E.5 Test results for projector switch-mode power supply

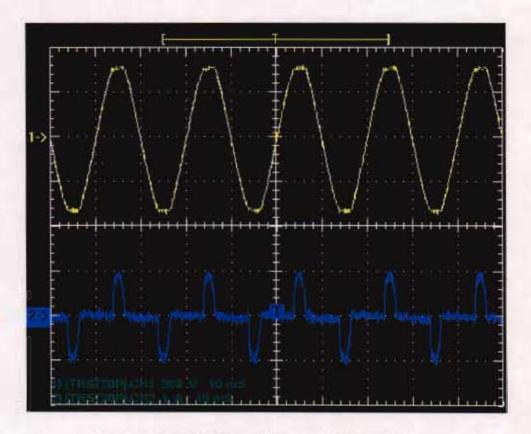


Figure 9 - Projector SMPS voltage and current waveforms

The full results obtained are:

Voltage = 234.30 V

Current = 400.21 mA

True Power = 61.723 W

Voltage **THD** = 3.083 %

Current THD = 105.704 %

Power Factor = 0.658

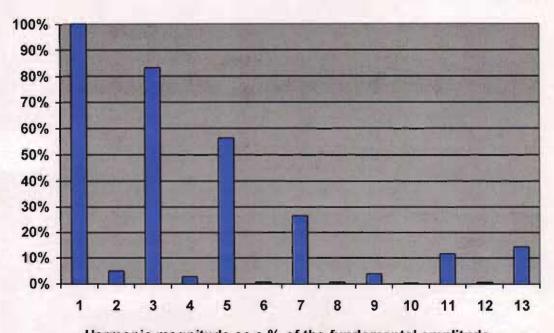
Displacement PF = -5.2343

Apparent Power = 93.770 VA

Reactive Power = 70.591 VAR

Harm No.	Freq.	Voltage RMS	Voltage % of Fund.	Voltage Phase	Current RMS	Current % of Fund.	Current Phase
Fund.	50.025 Hz	233.88 V	100.00 %	0.0000	269.09mA	100.00 %	0.0000
2 nd	100.05 Hz	1.7425 V	0.745 %	160.79	13.514mA	5.022 %	178.12
3 rd	150.08 Hz	2.1343 V	0.913 %	92.520	223.61mA	83.099 %	5.3795
4 th	200.10 Hz	632.69mV	0.271 %	65.086	7.6760mA	2.853 %	49.235
5 th	250.13 Hz	5.9258 V	2.534 %	-6.3826	151.61mA	56.342 %	-166.58
6 th	300.15 Hz	556.16mV	0.238 %	82.072	2.0291mA	0.754 %	-126.69
7 th	350.18 Hz	2.4840 V	1.062 %	-177.80	71.265mA	26.484 %	16.600
8 th	400.20 Hz	286.58mV	0.123 %	163.45	1.9861mA	0.738 %	78.378
9 th	450.23 Hz	1.2497 V	0.534 %	6.7616	10.532mA	3.914 %	155.76
10 th	500.25 Hz	588.62mV	0.252 %	-98.317	853.95uA	0.317 %	-167.22
11 th	550.28 Hz	447.09mV	0.191 %	-94.783	31.409mA	11.672 %	-128.96
12 th	600.30 Hz	99.350mV	0.042 %	-65.529	2.0117mA	0.748 %	-45.942
13 th	650.33 Hz	417.74mV	0.179 %	84.343	38.548mA	14.325 %	48.792



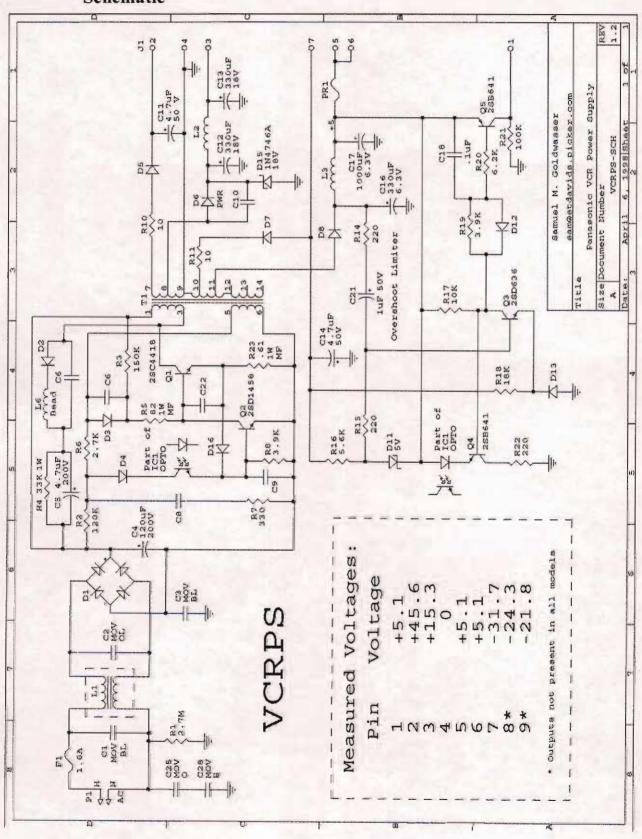


Harmonic magnitude as a % of the fundamental amplitude

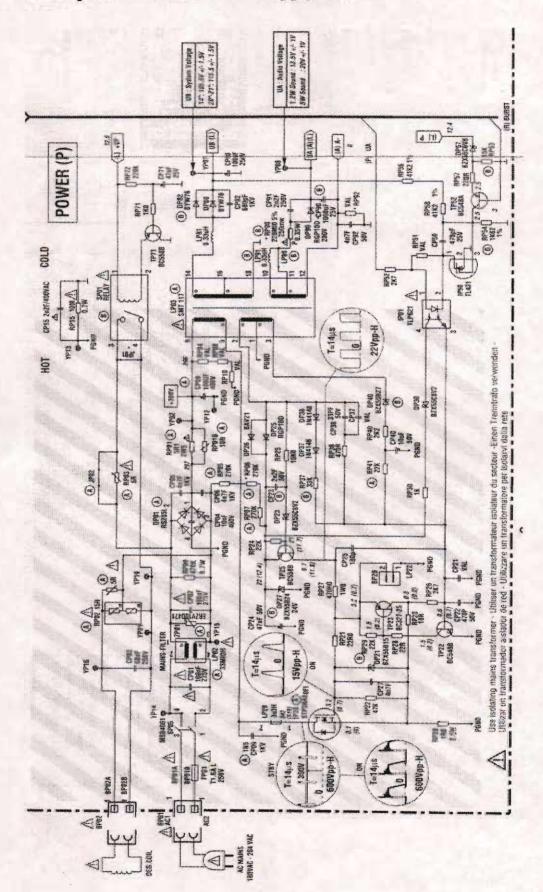
Harmonic No.	3 rd	5 th	7 th	9 th	11 th	13 th
Standard Limit [mA]	209.86	117.27	61.72	30.86	21.60	18.28
Recorded Level [mA]	223.61	151.61	71.265	10.532	31.409	38.548

Appendix F: Additional Television / VCR Schematics

F.1 Panasonic Video Cassette Recorder Switch-Mode Power Supply Schematic

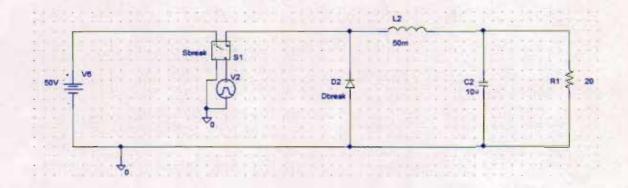


F.2 Thompson Television Power Supply Circuit

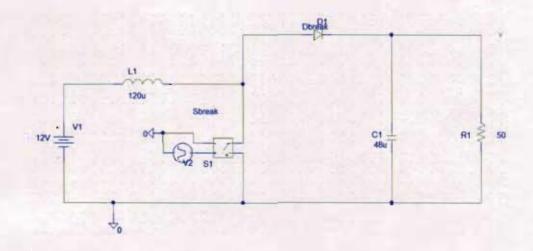


Appendix G: PSpice Simulation Circuit Files

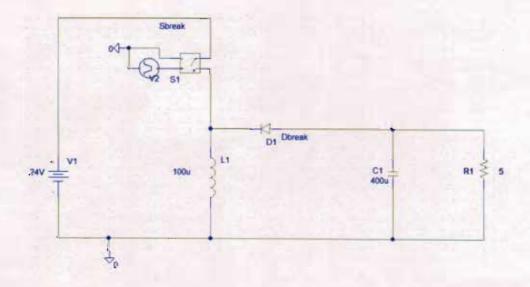
G.1 PSpice Schematics Buck Converter Circuit



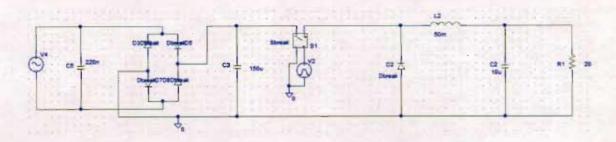
G.2 PSpice Schematics Boost Converter Circuit



G.3 PSpice Schematics Buck-Boost Converter Circuit



G.4 PSpice Schematics AC-to-DC converter with buck output filter



G.5 SMPS Example Voltage Dip Simulation circuit configurations and results

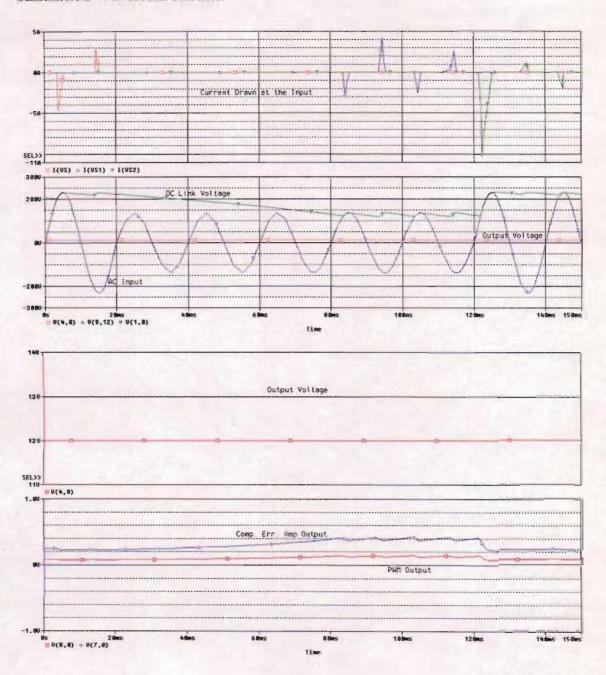
Ex.1: Voltage Dip at 40 % for 100 ms commencing at phase angle of 0°

Circuit Input File:

```
AC-DC Switch-Mode Power Supply Circuit for Voltage Dip Tests
******* Test 1 40% 100ms 0 degrees **********
********* CIRCUIT AND CONTROL PARAMETERS *******
.PARAM Vm = 230 F = 50
.PARAM CFILTER = 150uF
.PARAM ICC = \{0.9*Vm\}
.PARAM Vref = 12
.PARAM L = 100UH
                     rL = 2
.PARAM C = 80UF
                    rC = .6
.PARAM RLOAD = 5
.PARAM Vp = 3 ; (peak of ramp in modulator)
.PARAM R1 = 1K R2 = 33K C1= 1.45nF C2 = 161pF ;error amplifier parameters
*********** CIRCUIT DESCRIPTION ************
SW 9 10 SCONT 12 SMOD
.MODEL SMOD VSWITCH (RON=.001)
VPULSE SCONT 12 PULSE(0 5 0 1N 1N 19.99M)
VS 10 12 SIN (0 (Vm) (F))
SW1 9 11 SCONT1 12 SMOD1
.MODEL SMOD1 VSWITCH (RON=.001)
VPULSE1 SCONT1 12 PULSE(0 5 20M 1N 1N 99.99M)
VS1 11 12 SIN (0 {0.6*Vm; {F})
SW2 9 13 SCONT2 12 SMOD2
.MODEL SMOD2 VSWITCH (RON=.001)
VPULSE2 SCONT2 12 PULSE(0 5 120M 1N IN 199.99M)
VS2 13 12 SIN (0 {Vm} {F})
D1 9 1 DMOD
D2 12 1 DMOD
D3 0 9 DMOD
D4 0 12 DMOD
C1 1 1S {CFILTER} IC={ICC}
RC1 1S 0 0.5
R8 1 0 180000
XSWITCH 1 0 2 8
                    SWITCH
rL 2 3 {rL}
L 3 4 (L) IC={Vref/RLOAD}
```

```
rC 4 5 {rC}
C 5 0 {C} IC={Vref}
R 4 0 {RLOAD}
XCOMP 4 6 7 COMP
                    ; compensated error amplifier
Vref 6 0 (Vref)
XMOD 7 8 MODULATOR ; PWM controller
******* R-C SNUBBERS TO HELP WITH PSPICE CONVERGENCE ****
.SUBCKT SNUB 1 2
RSNUB 1 3 10000
CSNUB 3 2 .1NF
. ENDS
XSNUB1 9 1 SNUB
XSNUB2 12 1 SNUB
XSNUB3 0 9 SNUB
XSNUB4 0 12 SNUB
******* COMPENSATED ERROR AMPLIFIER SUBCIRCUIT ******
.SUBCKT COMP 1 5 3
*TYPE 2 COMPENSATING NETWORK 1=INPUT; 5=+ (NONINVERTING INPUT); 3=OUTPUT
R1 1 2 {R1}
R2 4 3 {R2}
C1 2 4 {C1}
C2 2 3 {C2}
RIN 2 5 1E6
EAMP 3 0 TABLE \{V(5,2)\}\ (-15U,-15)\ (15U,15)\ ; saturation at +/- 15 volts
. ENDS COMP
******* PWM CONTROLLER SUBCIRCUIT *********
.SUBCKT MODULATOR 1 2
*pulse-width modulator -- converts amplified error to duty ratio
RX 1 0 1G
EMOD 2 0 TABLE {V(1)/Vp} (0,0) (1,1)
RY 2 0 1G
.ENDS MODULATOR
****** AVERAGED SWITCH MODEL SUBCIRCUIT INCL. DIODE*******
* VORPERIAN'S SWITCH MODEL
.SUBCKT SWITCH A P C D
GAP A X VALUE {V(D)*I(VC)}
ECP X P VALUE={V(D)*V(A, 0)}
VC X C 0
RCONV D 0 1G
.ENDS SWITCH
. PROBE
.TRAN 10u 150m UIC
.MODEL DMOD D; Default diode
```

Simulation Waveform Results:



Ex.2: Voltage Dip at 85 % for 1000 ms at phase angle of 0° using 1000 μF input capacitor

```
.PARAM L = 100UH rL = 2
.PARAM C = 80UF
                     rC = .6
.PARAM RLOAD = 5
.PARAM Vp = 3 ; (peak of ramp in modulator)
.PARAM R1 = 1K R2 = 33K C1 = 1.45nF C2 = 161pF ; error amplifier parameters
************ CIRCUIT DESCRIPTION *************
SW 9 10 SCONT 12 SMOD
.MODEL SMOD VSWITCH (RON=.001)
VPULSE SCONT 12 PULSE(0 5 0 1N 1N 39.99M)
VS 10 12 SIN (0 {Vm} {F})
SW1 9 11 SCONT1 12 SMOD1
.MODEL SMOD1 VSWITCH(RON=.001)
VPULSE1 SCONT1 12 PULSE(0 5 40M 1N 1N 999.99M)
VS1 11 12 SIN (0 {0.15*Vm} {F})
SW2 9 13 SCONT2 12 SMOD2
.MODEL SMOD2 VSWITCH (RON=.001)
VPULSE2 SCONT2 12 PULSE(0 5 1040M 1N 1N 199.99M)
VS2 13 12 SIN (0 {Vm} {F})
D1 9 1 DMOD
D2 12 1 DMOD
D3 0 9 DMOD
D4 0 12 DMOD
C1 1 1S {CFILTER} IC={ICC}
RC1 1S 0 0.5
R8 1 0 180000
XSWITCH 1 0 2 8
                   SWITCH
rL 2 3 {rL}
L 3 4 {L}
           IC={Vref/RLOAD}
rC 4 5 {rC}
C 5 0 {C} IC={Vref}
R 4 0 {RLOAD}
XCOMP 4 6 7 COMP ; compensated error amplifier
Vref 6 0 {Vref}
XMOD 7 8 MODULATOR ; PWM controller
******* R-C SNUBBERS TO HELP WITH PSPICE CONVERGENCE ****
.SUBCKT SNUB 1 2
RSNUB 1 3 10000
CSNUB 3 2 .1NF
. ENDS
XSNUB1 9 1 SNUB
XSNUB2 12 1 SNUB
XSNUB3 0 9 SNUB
XSNUB4 0 12 SNUB
****** COMPENSATED ERROR AMPLIFIER SUBCIRCUIT ******
.SUBCKT COMP 1 5 3
*TYPE 2 COMPENSATING NETWORK 1=INPUT; 5=+ (NONINVERTING INPUT); 3=OUTPUT
R1 1 2 (R1)
R2 4 3 {R2}
C1 2 4 {C1}
C2 2 3 {C2}
RIN 2 5 1E6
EAMP 3 0 TABLE \{V(5,2)\}\ (-15U,-15)\ (15U,15)\ ; saturation at +/-\ 15\ volts
.ENDS COMP
******* PWM CONTROLLER SUBCIRCUIT ********
SUBCKT MODULATOR 1 2
*pulse-width modulator -- converts amplified error to duty ratio
RX 1 0 1G
EMOD 2 0 TABLE \{V(1)/Vp\} (0,0) (1,1)
RY 2 0 1G
.ENDS MODULATOR
```

```
******** AVERAGED SWITCH MODEL SUBCIRCUIT INCL. DIODE******

* VORPERIAN'S SWITCH MODEL
.SUBCKT SWITCH A P C D
GAP A X VALUE {V(D)*I(VC)}
ECP X P VALUE={V(D)*V(A,0)}
VC X C 0
RCONV D 0 1G
.ENDS SWITCH
```

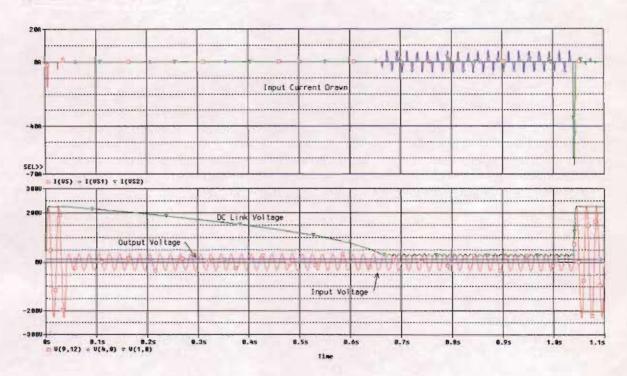
. PROBE

.TRAN 10u 1100m UIC

.MODEL DMOD D; Default diode

.END

Simulation Waveforms:



Appendix H: ESB Network Model: Underground Cable and Overhead Line data

Underground Cable Data

Resistance (Ω per km)	0.215 (positive sequence) 0.788 (zero sequence)
Inductance (mH per km)	0.360 (positive sequence) 0.694 (zero sequence)
Capacitance (µF per km)	0.26

Resistance (Ω per km)	0.572 (positive sequence)
	1.320 (zero sequence)
Inductance (mH per km)	0.420 (positive sequence)
The second secon	1.149 (zero sequence)
Capacitance (µF per km)	0.184

Overhead Line Data

Resistance (Ω per km)	0.490 (positive sequence) 0.660 (zero sequence)
Inductance (mH per km)	1.019 (positive sequence) 6.462 (zero sequence)
Capacitance (µF per km)	0.02

25 mm ² 20 kV aluminium overhe	ad conductor
Resistance (Ω per km)	1.540 (positive sequence) 1.700 (zero sequence)
Inductance (mH per km)	1.082 (positive sequence) 6.525 (zero sequence)
Capacitance (µF per km)	0.02

25 mm ² 400 V aluminium overhe	ad conductor
Resistance (Ω per km)	0.570 (positive sequence) 1.330 (zero sequence)
Inductance (mH per km)	0.318 (positive sequence) 0.987 (zero sequence)
Capacitance (µF per km)	0.182

Appendix I: ESB Network Model Surge Simulation
Results

ESB Network Surge Simulation Results - Light loading with 26 kA lightning

		Test 1	Test 2	Test 3	Test 4	Test 5	Test6	Test 7	Test8	Test9	Test 10	Test 11	14	Test 13
Lightly Loaded	Nominal Peaks	26kA Neg. Lgt Src	26kA Neg. Lgt Src+Arr	26kA Neg. Lgt Line	Z6kA Neg Lgt Line+Arr	26kA Pos. Lgt Src	26kA Pos. Lgt Src+Arr	26kA Pos. Lgt Line	26kA Pos. Lct Line+Air	26kA Neg. Lgt Ard	26kA Neg. Lg¢ Ard+Arr	Sw Surge Src	Svc	Sw Surge Fuse
age					100	1			7		100000	185		
422	16.1 kV	96.7 kV	94 5 KV	153 kV	VX 69	97.5 kV	945 KV	154 KV	70 KV	149.5 kV	66.6 kV	1		1
M	16.1 KV	144 KV	138.5 kV	234 KV	92.2 KV	144 KV	138.5 kV	234 KV	92.6 KV	198 KV	VA 6.98	1		17.7 kV
Vspicer	16.1 kV	178 KV	77.9 KV	580 kV	82 KV	179 KV	78.2 KV	580 KV	819KI	395.6 kV	68 KV	1	SAME	19.1 KV
Movine	2	165 KV	74.5 KV	1.968 kV	87 KV	166 kV	74.5 KV	1,968,5kV	87 kV	989.5 kV	71.9 KV	1		-145.3 kV
Vkilcam	-	153 KV	74 KV	1.472 kV	89 KV	153KV	745 KV	1,472 kV	89 kV	1,405 KV	75.3 kV	1	AS	17.2 KV
Vard	16.1 kV	150 KV	74 KV	1.030 KV	84 2 KV	150 kV	745 KV	1,036.5kV	842KI	8290 kV	213.5 kV	1		16.7kV
Vrugby	1	156 KV	74 KV	1,214 KV	86.5 kV	157 KV	74.5 KV	1,216 kV	86.5 KV	1,139 kV	77.1 kV	1	WITHOUT	1
Vbal	16.1 KV	166 KV	74.5 kV	1,545 kV	77.5 KV	167 KV	74.5 kV	153 kV	775KV	1,528 kV	77.6 kV	1		1
VspicerH1	0.325 KV	1 709 kV	0.988 kV	5.61 kV	1.01 kV	1.71 kV	0 99 kV	5.61 kV	1.01 kV	4.18 KV	0.832 kV	-	ARR.'S	1
WoowneH1	0.325 KV	1.816 KV	0 953 KV	20.9 KV	1.13 KV	1.82 KV	0.955 kV	20.9 KV	1 13 KV	10.87 KV	0.89 kV	-		0.794 KV
VkilcarnH1	0.325 kV	1.756 KV	0.94 KV	14.8 kV	1.09 KV	1.76 KV	0.955 kV	14.8 KV	1.09 KI	13.9 kV	0.962 kV	1	DONOT	1
VardH1	0 325 kV	1.75 KV	0 936 KV	10.89 kV	1 05 KV	1.76 KV	0.955 kV	10.9 KV	1.05 KV	47 KV	1.13 kV	1		1
VrugbyH1	0.325 kV	1.825 kV	0 94 KV	13.5 KV	1.09 kV	1.83 KV	0.955 kV	13.4 KV	1 09 KV	12.6 kV	1 1 1 1 1	1	EXCEED	
VbalH1	0.325 kV	1.93 KV	0.947 KV	17.1 kV	0.994 kV	1.94 KV	0.617 kV	17.1 kV	0.995 k/	17.1 kV	0.98 kV	1		0.363 kV
VspicerH2	0.325 kV	0.56 kV	0.56 kV	0.74 kV	0.579 kV	0.612 kV	0.668 kV	0.647 kV	0.651 RV	0.619 kV	0.579 kV	0.52 KV	ARR.'S	1
WoowneH2	0.325 kV	0.58 kV	0.59 kV	2.48 kV	0.598 kV	0.666 KV	0.668 kV	0.693 kV	0.685 kV	2.18 KV	0.601 kV	0.56 kV		-0.533 KV
VkikarnH2	0.325 kV	0.592 KV	0.59 kV	2.87 kV	0.61 kV	0.666 KV	0.668 kV	0.738 kV	0.706 KY	2.74 KV	0.6165 kV	0.54 KV	RATING	1
VardH2	0.325 kV	0.593 kV	0.59 kV	2.89 kV	0.612 kV	0.666 kV	0.668 kV	0.705 KV	0 708 KV	2.75 KV	0.62 kV	0.583 kV	N. SH. CAN	1
VrugbyH2	0.325 kV	0.592 kV	0.589 kV	-3.52 kV	0.61 kV	0.666 KV	0.668 kV	0.715 kV	0.706 kV	-3.71 KV	0.618 kV	0.565 kV		-
VbalH2	0.325 kV	0.59 kV	0.59 kV	4.74 KV	0.61 kV	0.666 kV	0.668 kV	0.76 kV	0.706 kV	4.76 KV	0.619 kV	0.604 kV		1
Current		4	2460			- 20		The same of the same	100000	The same of the same of				
ls s	95 A	2,600 A	26,100 A	45,600 A	17.800 A	26,000 A	26,000 A	45,800 A	-18,2004	-44,500 A	-17,200 A	-3,120 A		-1,230 A
11	95 A	13,400 A	13,000 A	44,800 A	17.800 A	19,000 A	19,000 A	-45,000 A	-18,2004	-44 200 A	-17,200 A	-3,120 A		-1,230 A
Ispicer	6A	33,800 A	3.370 A	1.410A	5,180 A	9,940 A	9.930 A	3,820 A	5,180 4	608 A	564 A	-360 A	10 mm	-109 A
Iboyne	44	970 A	965 A	1,090 A	14,400 A	2,070 A	965 A	2,690 A	14,400 A		434 A			820 A
kilcarn	48 A	5,920 A	5 750 A	7,040 A	21,400 A	8,020 A	5.750 A	9,440 A	21,400 A	5.700 A	5,260 A	-1.460 A		-630 A
lard	24 A	2,900 A	2,800 A	3,440 A	8,300 A	3,930 A	2,800 A	4.630 A	8,300 4		216,000 A			-311A
Irugby	12 A	1,540 A	1,480 A	1,830 A	13,200 A	2,090 A	1,480 A	2,660 A	13,200 A	1,770 A	1,890 A	-370 A		162 A
lp:sq	1.8 A	233 A	879 A	276 A	2.020 A	316A	879 A	432 A	2,060 4	268 A	2,050 A	-56 A	100	-24 A
Ispicer#1	22 A	945A	67.8 A	309 A	68.8 A	94.8A	678A	309 A	68.8 A	276.5A	57.15A	1		,
IboyneH1	13.2 A	32 A	28.6 A	254 A	28.8A	32.5A	28.6 A	254 A	29.1 A	138 A	27 A	/		1
KacarnH1	160 A	382 A	343 A	2230 A	350 A	393 A	343 A	2230 A	325.97	2160 A	340 A	1		-1
lardH1	80 A	192 A	172 A	866 A	175 A	197 A	172 A	869 A	176 A	3400 A	182 A	/		1
IrugbyH1	40 A	97.5 A	86.1 A	521A	88 A	98.8 A	86.1 A	521 A	882A	494 A	86.5 A	/		1
IbaH1	6A	152 A	13.2/6	96.6 A	13.2A	15.2A	132A	96.7A	132A	97.3A	13 A	1		1
IspicerH2	22 A	38.5 A	38 48 A	A 9 A	39 5 A	A 2 A	2R AR A	AAFA	AAAA	41 CA	7 8 DE	A 37C		1
					20.00	1774	20000	100	1	100	2000	27.72		

ESB Network Surge Simulation Results - Light loading with 100 kA/210 kA lightning

		183	71891	est 3	lest 4	lesto	128	lests	esty	lest 10	Test 11	14	est 13
Lighthy	Nominal	100kA	100kA	100KA	100kA	210kA	210KA	210KA	100ka	100kA	Sw Surga	_	Sw Surge
Loaded	Peaks	Neg. Lgt Src	Neg. Lgt Src+Arr	Neg. Lgt	Neg Lgt Line+Arr	Pos. Lgt Src	Pos. Lgt Line	Pos. Lgt Line+Arr	Neg. Lgt Ard	Neg. Lgt Ard+Arr	3	-,	Fise
909													
Vs	16.1 kV	326 kV	316 KV	527.4 KV	84.2 KV	673 KV	1,023 kV	100 KV	VA 8.003	73 KV			
VI	16.1 kV	507 kV	485 KV	831 KV	212.5 KV	1,048 kV	1,672 kV	341 KV	676.8 kV	73.4 KV			
Vspicer	16.1 kV	643 KV	VA 4.6	2,187 KV	91 1 kV	1,332 KV	4.573 kV	-102 KV	1,355 kV	74.5 KV			
Vboyne	16.1 KV	590 KV	83 KV	7,527 KV	94.5 KV	1,227 kV	15,777 KV	98.7 kV	3,744 kV	782 kV			
Vkilcam	16.1 KV	541 KV	81 kV	5,615 kV	96.5 kV	1,120 kV	11,778 KV	101 kV	5,344 kV	82.4 KV			
Vard	16.1 kV	529 KV	80 KV	3,695 kV	91.6 kV	1,096 kV	7,630 kV	96.6 kV	31,841 kV	415.5 kV			
Vnugby	16.1 kV	555 KV	80 kV	4,600 KV	1082 KV	1,153 kV	905 KV	131 KV	4,263 kV	82.8 kV			
Vbal	16.1 kV	594 KV	78.5 KV	5,820 kV	84.7 KV	1234 KV	12,175 kV	89.5 kV	5,833 kV	81 kV			
VspicerH1	0 325 kV	5.78 KV	117 KV	20.8 kV	1 12 kV	11.9 kV	43.4 kV	1.18 KV	12.7 KV	0.883 kV			
WhowneH1	0 325 kV	621 kV	1 03 kV	79.5 kV	125 kV	12 8 kV	167 kV	1387	41 kV	0 947 kV			
WkilcarnH1	0 325 KV	5.98 kV	0 996 kV	56.2 kV	1 18 KV	12.3 kV	117.7 KV	126 KV	48.9 KV	1.01 KV			
VardH1	0.325 kV	5.86 kV	VA 286 0	39.4 KV	1.17 KV	12.3 kV	82.5 KV	123 kV	180.3 KV	123 kV			
VrugbyH1	0.325 kV	6.25 kV	VA 86 0	42.8 kV	12 KV	12.8 kV	89.7 kV	127 KV	40.6 kV	1.03 KV			
VbalH1	0.325 kV	6.65 kV	0.973 kV	65 kV	117 KV	13.7 KV	127 kV	1.15 kV	65.1 kV	1.01 kV			
VspicerH2	0.325 KV	1.04 KV	0.738 kV	3.47 kV	0.773 kV	1.39 kV	4.67 kV	0 786 kV	3.76 kV	0.704 KV			
VboymeH2	0.325 kV	1.39 kV	0.805 kV	9.43 kV	0.835 KV	2.29 KV	15.1 KV	0.859 kV	10.9 kV	0.789 kV			
VkilcarnH2		1.63 kV	0.849 kV	11.5 kV	VA 088.0	2.82 kV	17.3 kV	0.910 kV	14.5 KV	0.846 kV			
VardH2	0.325 kV	-1.470 kV	0.852 kV	112 kV	0.890 kV	2.9 kV	18 KV	0.911 kV	15.7 kV	0.861 kV	55		
VrugbyH2	0.325 kV	1.78 kV	0.850 kV	14.5 kV	VM 068.0	3.06 KV	20.8 kV	0.910 kV	19 kV	0.854 KV	0.00		1000
VbalH2	0 325 KV	1.94 kV	0.852 kV	19.4 kV	0.890 KV	3.48 kV	24.5 kV	0.908 kV	24.4 kV	0.855 kV			
erit		100	A	100					1				
S	95 A	100 kA	100 KA	-170.3 KA	-30 kA	210 KA	-335.5 kA	-33 8 KA	-161 kA	-27.5 KA			
_	95 A	52.6 kA	68.3 kA	-16.7 kA	-30 kA	128 KA	-328.5 kA	-33.7 kA	-161 kA	-27.5 kA			
spicer	6 A	14.1 KA	56.5 kV	6.12 kA	24.1 KA	70.5 KA	26.9 KA	52.9 KA	2.69 kA	1.95 KA			
boyne	44	3.7 KA	6.92 KA	4.5 KA	57.7 KA	14.4 KA	19.6 KA	122 1 KA	2.02 kA	2.54 KA			
kilcarn	48 A	23.7 KA	178 kA	9.43 KA	85.9 KA	56.6 KA	66.5 KA	181.8 KA	24.8 KA	16.8 KA			
laro	24 A	1.0 KA	SOF	13.7 KA	A STATE	21.1 KA	32.6 KA	13.3 KA	23.2 KA	1,221 KA			
lbal	18A	0.909 kA	2.67 kA	1.2kA	9.22 KA	2.21kA	2.87 KA	23.3KA	1.10 KA	4.44 KA		- 3	100
coloor44	0.50	340.4	A 00	4 430 A	76.6	V 283	A 036 C	V V0	A 258	61.0		60 S 20	
H	V 9 6 P	A Se	V 000	0410	A CC	167 A	4 060 A	33.0	V 201	Vac			
linoyilei i	13.2 M	1 000 4	200	0 430 A	320 A	4 050 4	1,300 A	354 A	433 M	254 A			
-	W000	A CO.	1333 A	0,130 A	A010	A 170	A 0000 3	V 100	47,000 4	A1004			
IniohvH1	40 A	264 A	89 A	1 560 A	43A	514 A	3.240 A	A 29	1 500 A	20 A			
lball11	6.A	42A	13A	355A	13A	82 A	686 A	13A	358 A	13A	6000		775
spicerH2	22 A	71A	51 A	233A	53 A	95 A	313 A	54A	257 A	48A			
	1				-			1000					

ESB Network Surge Simulation Results - Full loading with 26 kA lightning

		Test 1	Test 2	Test 3	Test 4	Test 5	Test 6	Test 7	Test8	Test 9	Test 10	Test 11	14 14 M	Test 13
Lighthy	Nominal	Z6kA Neg. Lgt	Z6kA Neg. Lgt	26kA Neg. Lgt	26kA Neg Lgt	Z6kA Pos. Lgt	Z6kA Pos. Lgt	26kA Pos. Lgt	26kA Pos. Lút	26kA Neg. Lgt	26kA Neg. Lgt Ard+Arr	Sw Surge Src	Src	Sw Surge Fuse
Valence		2	200	2		2	20.05	1	2	2				ı
Ns.	1K 1 IV			153.2 kV								-		14.9 kVidio)
5	16 1 kV			233.6 KV								-		-23 KV
Vspicer	16.1 kV			580.5 KV								-	SAME	36.5 kV
Vboyne	16.1 kV	SAME										1		418 KV
Vkilcam	16.1 KV					OADING O	COADING OF THE TRANSFORMER	USFORMER	~			_	AS	-205 kV
Vard	16.1 kV	AS	SAME	A STATE OF THE REAL PROPERTY.								_		20 5 kV
Vrugby	16.1 KV			SAME								1	WITHOUT	20.9 KV
Vbal	16.1 KV	WITH	AS			HASLITTL	HAS LITTLE TO NO EFFECT ON	FECT ON				1		-223 KV
VspicerH1	A 205 LV			56 kV								1	S. ARA	O KAB LV
VbowneH1	VA 255 0	LIGHT	WITH									,		10.7 KV
WilcarnH1	0.325 KV					THE VOLT	THE VOLTAGE AND CURRENT	URRENT				1	DO NOT	0 344 KV
VardH1	0.325 KV	LOAD	LIGHT									1		0.353 KV
VrugbyH1	0.325 kV						PEAKS					1	EXCEED	0.362 kV
VbalH1	0.325 kV		LOAD	1								1		0.402 kV
VspicerH2	0.325 kV			0.738 kV	A PARTIE	SEEN ON	SEEN ON THEIRS OUTPUTS	UTPUTS	- 5			0.52 kV	ARR.'S	The Paris
VboyneH2	0.325 kV		FEW									0.56 kV		6.314
WilcarnH2	0.325 KV		VOLTS									0.54 kV	RATING	7
VardH2	0.325 kV											0.583 kV		-
VrugbyH2	0.325 kV		DECREASE								740	0.565 kV		1
/ballH2	0.325 kV					OADING OF	CADING OF THE TRANSFORMER	ISFORMER				0.604 kV	MARIE I	7
urrent														
S	118 A			-45,600 A								-3,120 A		-1870 A
=	118 A			-44,800 A		HASLITIC	HAS LITTLE TO NO EFFECT ON	FECT ON				-3.120 A		-1870 A
Ispicer	15A			14,200 A								-360 A		-231A
boyne	5A	SAME	4									-166 A		1098 A
IKBCarn	50 A	V	SAME			I LE VOL	HE VOLI AGE AND CURREN	CHARD				-1,460 A		4/3
lard	30 A	2	4				071470					-120 A		45/A
, and a	TD A	TANKE I	3				LEAKS					STUR		-248 A
Ibal	23A	WITH										-56 A		1376A
SpicerH1	22 A		WITH	309 A		SEEN ON	SEEN ON THEIRS OUTPUTS	JTPUTS	ľ			-		1
IboyneH1	13.2A	LIGHT										-		160 A
ikilcarnH1	160 A		LIGHT									1	100	
lardH1	80 A	LOAD										1		
IrugbyH1	40 A		LOAD									1		1
lbaH1	6A											1		
IspicerH2	22 A											27.6 A		
P. Chouse	4000													100