2003-01-01

Phase Balancing and Harmonic Mitigation for Large Electrical Loads

Hugh O'Kelly
Technological University Dublin

PHASE BALANCING AND HARMONIC MITIGATION FOR LARGE ELECTRICAL LOADS

Hugh O'Kelly, B.Sc. C.Eng. M.I.E.I.

Thesis for Master of Philosophy

Dublin Institute of Technology

Supervisors
Dr. Eugene Coyle, Mr. Michael Farrell

School
Kevin Street College, Dublin

2003

I certify that this thesis which I now submit for examination for the award of Master of Philosophy in Engineering, is entirely my own work and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

This thesis was prepared according to the regulations for postgraduate study by research of the Dublin Institute of Technology and has not been submitted in whole or in part for an award in any other Institute or University.

The Institute has permission to keep, to lend or to copy this thesis in whole or in part, on condition that any such use of the material of the thesis be duly acknowledged.

Signature _____

Date _____

ABSTRACT

This thesis describes the development and implementation of new solutions to the power quality problems associated with large unbalanced and non-linear loads. The thesis was undertaken in the context of the fine glass industry and the development work was carried out at three production plants belonging to a world leading fine glass producer.

In the process of fine glass production, furnaces are used to melt the silica mix into a liquid of treacle consistency. These furnaces are generally enclosed, except for several small orifices about 50 mm in diameter, which are located around their perimeter. Through these openings, glass blowers draw a working portion of this treacle like substance, using a hollow tube. By the use of a blowing and moulding technique the desired product is shaped.

The process of manufacture of fine glass products is presently undergoing change due to the introduction of process automation by the leading manufacturers. Robotic machines are now replacing glass-cutters and craft-blowers.

Fine glass producers traditionally used many small gas or oil fired furnaces in order to allow blowers sufficient access and work space. Robotic production involves different requirements and this has given rise to a radical redesign of furnace construction.

Large furnaces are now being constructed, each one capable of meeting a major portion of the requirements of one major producer. These furnaces consist of a multi-channel layout, arranged in order to facilitate the various types of robotic connection required to produce a variety of products.

Electricity is being used to achieve the critical temperature and viscosity necessary for good quality control. New electrical problems are being encountered in the area of electrical supply, operation and control. Among these are the issues of electrical phase balancing and the generation of harmonic distortion on the connected electrical network. These problems can be so serious as to cause the entire furnace system to be inherently

unreliable in normal operation. The possibility of system failure is serious and the consequential damages could run into many millions of Euro. This thesis aims to address and solve some of these design problems.

The thesis describes and compares two new and untried approaches to the balancing of large two-phase loads across three phases and shows how these have been designed and implemented. It also describes a new design method and computer programme for the construction of harmonic filters to solve the harmonic problems associated with this type of load.

ACHNOWLEGDGEMENTS

The development work described in this thesis was undertaken at the Waterford Crystal plant in Butlerstown, Waterford City. I would like to thank Waterford Crystal for the use of the 30kW test furnace, for this purpose. I would also like to thank Mr. Michael O'Brien and Mr. Ernie Rice of Waterford Crystal Ltd., for their faith and forbearance in embracing these new ideas; Dr Eugene Coyle and Mr Michael Farrell of DIT for their time and support while developing this thesis; my good friend Mr Liam Campbell, ESB (retired) for his advice and encouragement during the project. I would especially like to thank my wife Mary for her patients and support.

ABSTRACT

This thesis describes the development and implementation of new solutions to the power quality problems associated with large unbalanced and non-linear loads. The thesis was undertaken in the context of the fine glass industry and the development work was carried out at three production plants belonging to a world leading fine glass producer.

In the process of fine glass production, furnaces are used to melt the silica mix into a liquid of treacle consistency. These furnaces are generally enclosed, except for several small orifices about 50 mm in diameter, which are located around their perimeter. Through these openings, glass blowers draw a working portion of this treacle like substance, using a hollow tube. By the use of a blowing and moulding technique the desired product is shaped.

The process of manufacture of fine glass products is presently undergoing change due to the introduction of process automation by the leading manufacturers. Robotic machines are now replacing glass-cutters and craft-blowers.

Fine glass producers traditionally used many small gas or oil fired furnaces in order to allow blowers sufficient access and work space. Robotic production involves different requirements and this has given rise to a radical redesign of furnace construction.

Large furnaces are now being constructed, each one capable of meeting a major portion of the requirements of one major producer. These furnaces consist of a multi-channel layout, arranged in order to facilitate the various types of robotic connection required to produce a variety of products.

Electricity is being used to achieve the critical temperature and viscosity necessary for good quality control. New electrical problems are being encountered in the area of electrical supply, operation and control. Among these are the issues of electrical phase balancing and the generation of harmonic distortion on the connected electrical network. These problems can be so serious as to cause the entire furnace system to be inherently

unreliable in normal operation. The possibility of system failure is serious and the consequential damages could run into many millions of Euro. This thesis aims to address and solve some of these design problems.

The thesis describes and compares two new and untried approaches to the balancing of large two-phase loads across three phases and shows how these have been designed and implemented. It also describes a new design method and computer programme for the construction of harmonic filters to solve the harmonic problems associated with this type of load.

ACHNOWLEGDGEMENTS

The development work described in this thesis was undertaken at the Waterford Crystal plant in Butlerstown, Waterford City. I would like to thank Waterford Crystal for the use of the 30kW test furnace, for this purpose. I would also like to thank Mr. Michael O'Brien and Mr. Ernie Rice of Waterford Crystal Ltd., for their faith and forbearance in embracing these new ideas; Dr Eugene Coyle and Mr Michael Farrell of DIT for their time and support while developing this thesis; my good friend Mr Liam Campbell, ESB (retired) for his advice and encouragement during the project. I would especially like to thank my wife Mary for her patients and support.

CHAPTER 1
INTRODUCTION

1.1 Background

The manufacture of fine glass products by such companies as Waterford Crystal of Ireland, Stuart Crystal of UK, Swarovski of Austria, Atlantis of Portugal, is currently in the process of being automated, with skills transferred from craft workers to robotic production systems. The process also involves the replacement of the traditional pot furnaces used by the glass blowers, with large industrial electrically heated units having power ratings in the region of 1 MW to 3 MW.

These furnaces are constructed using a glass-based refractory brick and the glass is generally kept in a molten state at 1,150 degrees Centigrade by means of resistance heating. To achieve this, a large current is passed through the molten glass. If power to the furnace fails, the contents begin to cool down immediately. As the temperature reduces the glass resistance increases, reducing its ability to absorb power. A point is quickly reached (quarter to half an hour depending on furnace size) where the molten glass fuses with the refractory brick. Once this happens the process becomes irreversible and the whole furnace turns into a solid glass block. The only solution at this point is to break up and remove the glass block and rebuild the entire furnace. Such a failure would result in major rebuild costs together with consequent loss of production and market. The rebuild cost alone, of a typical 1 Mega-Watt furnace is estimated to be in the region of 10 million Euro.

In order to reduce the risk of such a failure, electric glass furnace manufacturers and users have examined and treated weaknesses in the construction and within the electrical supply configuration. One of the major remaining weaknesses is the fact that these furnaces used two-phase electricity for reasons of enhanced current direction control and consistency of glass viscosity. A significant risk of power failure is introduced due to this requirement, as will be described in this thesis. The furnace load is also non-linear in nature, due to temperature control by thyristor switching. This gives rise to risks associated with high harmonic distortion. Under circumstance that

will be described in this thesis, failure of essential ancillary equipment and the supply system itself can result directly from these arrangements.

The question of risk analysis and reduction, relating to power supply, has occupied the minds of numerous engineers in the glass industry, and solutions have hinged on the issue of balancing a two-phase load over three phases, and removing the harmonic distortions caused by the methods of temperature control.

1.2 Aims and Objectives

The aims of this thesis are;

I. To identify and treat the issues of electrical load unbalance and harmonic distortion which are causing production limitation and reliability problems for the leading fine glass production manufacturers

II. To design construct and compare two new types of electrical load balancer for use with large industrial loads

III. To design a method and new programme for use in the specification and construction of suitable harmonic filters for use with large non-linear loads

IV. To describe methods by which these solutions can easily be repeated.

1.3 Method of Approach

This thesis originated from a request to the author for practical solutions to an industrial problem. The method and approach to developing these solutions and writing this thesis can best be illustrated diagrammatically as shown in Figure 1.1.

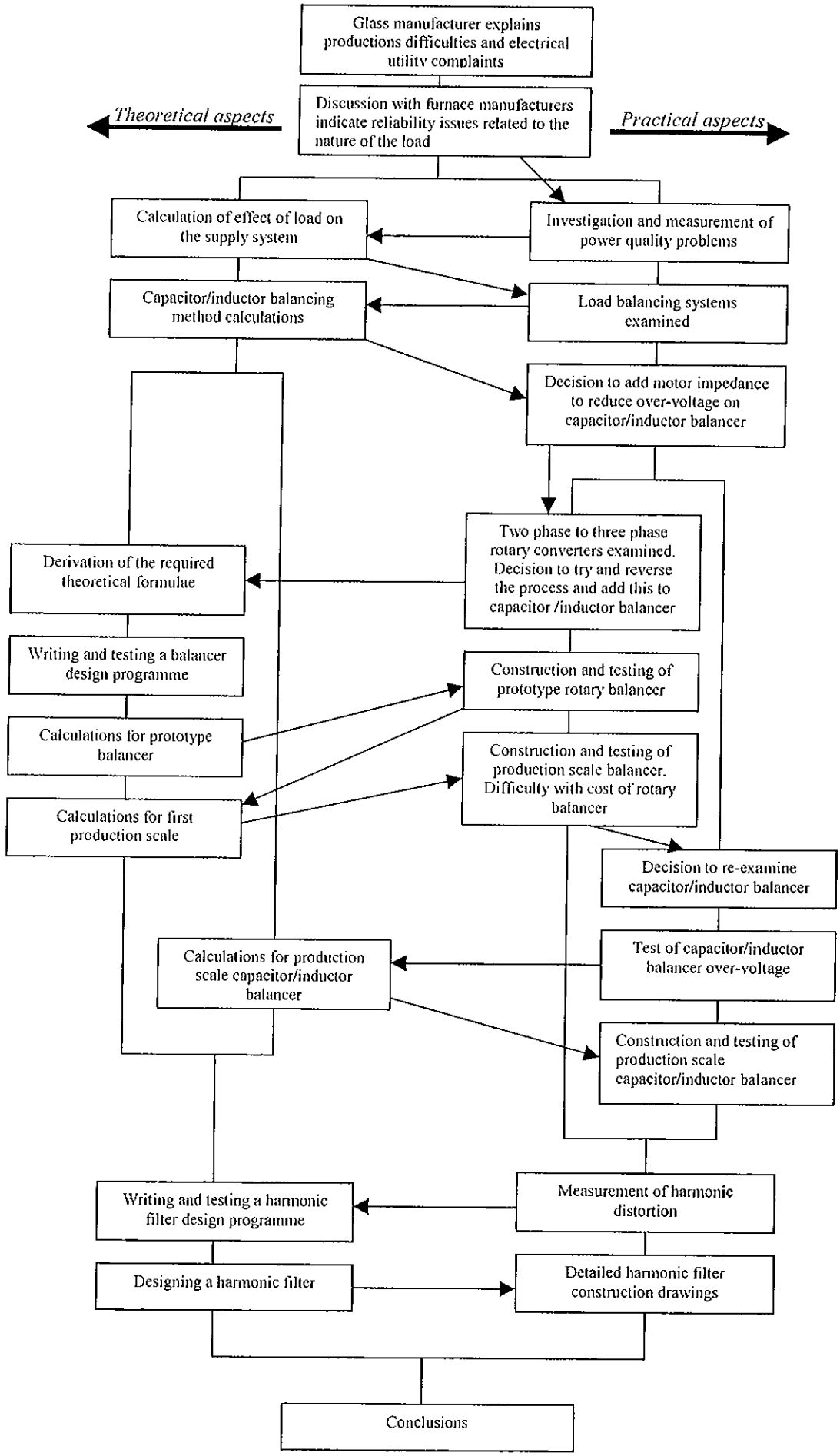


Figure 1.1 Method of Approach

CHAPTER 2
NECESSITIES FOR A GOOD QUALITY OF ELECTRICAL SUPPLY.

2.1 Voltage balance issues

AC electrical power is supplied to most industrial and commercial customers in the form of three-phase electricity. A large portion of this delivered power is consumed by three-phase machines, which are designed to operate with a supply of balanced three-phase voltage. Some allowance is made for the fact that the voltage may not always be perfectly balanced, and this will be discussed later. Some equipment, particularly motors and generators, are normally fitted with protection relays which will cause tripping in the event of the voltage or current unbalance exceeding a pre-set limit. The purpose of this protection is to prevent overheating and damage to three-phase machinery, resulting from this unbalance.

While the supply utilities may generate a three-phase balanced voltage, the load may introduce unbalance. For instance any current flow arising from active power consumption will result in a voltage drop at the terminals of the machinery. If the power is consumed unequally across the three phases, the voltage drop will also be unequal. This will result in an unbalance voltage system at the equipment terminals. This effect can be shown from the following calculation.

Unbalance Calculation

The following calculation illustrated the effect on voltage balance of connecting a 600 kW resistive load, across two phases of a previously balanced three-phase supply voltage of 400 volts, having a typical short circuit power of 16 MVA.

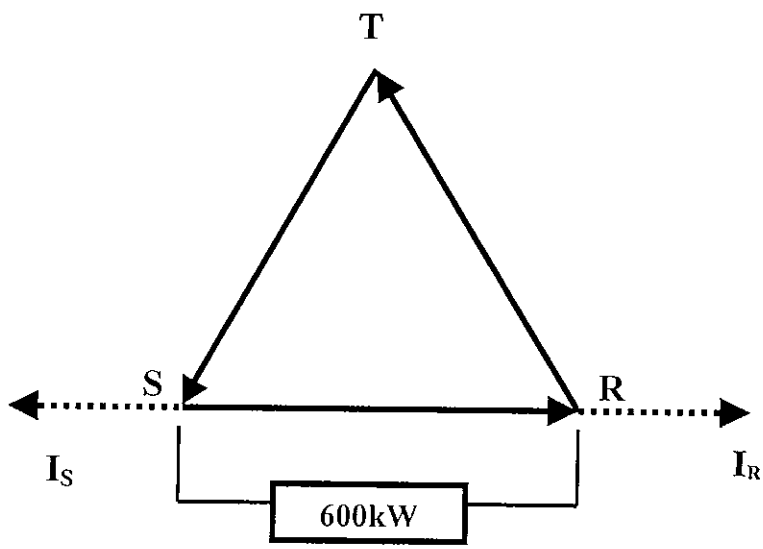


Figure 2.1 A vector diagram of the load.

Assuming for the sake of this example that the load is connected between phases R and S and the phase sequence is RST, as shown in Figure 2.1.

Then $I_R = I_{LOAD} = 1500$ A (1)

and $I_S = -I_R = -1500$ A (2)

According to the theory of symmetrical component analysis, any set of three-phase voltages or currents can be represented by the sum of its phase sequence components, positive, negative and zero.

$\therefore \quad I = I_1 + I_2 + I_0$

Where I_1 = Positive phase sequence currency

I_2 = Negative phase sequence current,

I_0 = Zero phase sequence current.

Where no neutral is connected the zero phase sequence component may be ignored. This applies to the above example and voltage unbalance will be expressed in terms of positive and negative sequence components only.

$\therefore \quad I = I_1 + I_2$

From the theory of symmetrical component analysis

$I_R = I_1 + I_2$ (3)

$I_S = \alpha^2 I_1 + \alpha I_2$ (where α the 120degree operator $= -0.5 + j\frac{\sqrt{3}}{2}$)

and $I_T = \alpha I_1 + \alpha^2 I_2$

From equation (1) $I_R = 1500 + j0$

Since the load is connected between R and S, zero current flows in T phase

$I_T = \alpha I_1 + \alpha^2 I_2 = 0$

$\therefore \quad I_1 = -\alpha I_2$ (4)

Substituting in (4) in (3)

$I_R = 1500 + j0 = -\alpha I_2 + I_2$

$= I_2(1 - \alpha)$

$\therefore \quad I_2 = 1500 \div (1 - \alpha) \quad = 750 + j433$ amps (5)

and $I_1 = -\alpha \times I_2 \quad = 750 - j433$ amps (6)

$\therefore \quad I_{R1} = \quad 750 - j433$

$I_{S1} = -750 - j433$

$I_{T1} = \quad 0 + j866$

$I_{R2} = \quad 750 + j433$

$I_{S2} = -750 + j433$

$I_{T2} = \quad 0 - j866$

Calculating the voltage drop due to the supply impedance

$\Delta V_1 = I_1 \times Z_{system}$

$\Delta V_2 = I_2 \times Z_{system}$

Deriving the phase sequence components of ΔV

$\Delta V_R = \Delta V_1 + \Delta V_2$

$\Delta V_S = \alpha^2 \Delta V_1 + \alpha \Delta V_2$

$\Delta V_T = \alpha V_1 + \alpha^2 \Delta V_2$

Assuming the short circuit power is largely inductive at 16 MVA

$Z = V^2 \div P = 400^2 \div 16 \times 10^6 = 0.01\ \Omega$

i.e. $Z = 0 + j0.01\ \Omega$

From (5) above $I_1 = 750 - j433$ amps

From (6) above $I_2 = 750 + j433$ amps

$\therefore \quad \Delta V_1 = (0 + j0.01)(750 - j433) = 4.33 + j7.5$

and $\Delta V_2 = (0 + j0.01)(750 + j433) = -4.33 + j7.5$

Deriving the phase sequence components of ΔV

$\Delta V_R = \Delta V_1 + \Delta V_2 = 0 + j15$

$\Delta V_S = \Delta \alpha^2 V_1 + \alpha \Delta V_2 = 4.33 - j7.5 - 4.33 - j7.5 = 0 - j15$

$\Delta V_T = \alpha \Delta V_1 + \alpha^2 \Delta V_2 = -8.66 - j0 + 8.66 - j0 = 0$

Looking at the loaded and unloaded voltage vector systems, Figures 2.2 and 2.3;

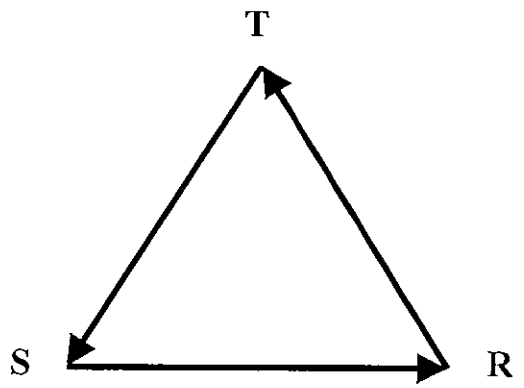


Figure 2.2 Unloaded System

$V_{RS} = 400 + j0$

$V_{ST} = -200 - j346.4$

$V_{TR} = -200 + j346.4$

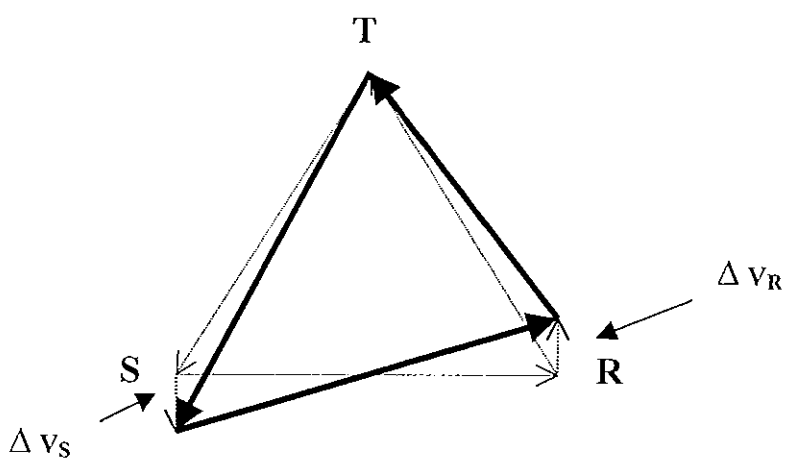


Figure 2.3 Loaded System

Loaded V_{RS} = unloaded $V_{RS} + \Delta V_R - \Delta V_S$

$= (400 + j0) + (0 + j15) - (0 - j15)$

$= 400 + j30$

Loaded V_{ST} = unloaded $V_{ST} + \Delta V_S - \Delta V_T$

$= (-200 - j346.4) + (0 - j15) - 0$

$= -200 - j361.4$

$$\text{Loaded } V_{TR} = \text{unloaded } V_{TR} + \Delta V_T - \Delta V_R$$
$$= (-200 + j346.4) + 0 - (0 + j15)$$
$$= -200 - j331.4$$

Deriving the positive and negative phase sequence components of the revised voltage system;

$$V_1 = (V_{TR} - \alpha^2 V_{RS})/3/\alpha$$
$$= \{(-200 - j361.4 - \alpha^2(400 + j30)\}/3/\alpha$$
$$= 204.33 + j107.97$$

$$|V_1| = 231.10 \text{ volts}$$

$$V_2 = (V_{TR} - \alpha V_{RS})/3/\alpha$$
$$= \{(-200 + j331.4 - \alpha(400 + j30)\}/3/\alpha$$
$$= -4.33 - j7.50$$

$$|V_2| = 8.66 \text{ volts}$$

Therefore the percentage negative phase sequence voltage is given by;

$$V_2/V_1\% = 3.75\ \%$$

Any other three-phase machinery connected at this point will also experience this level of voltage unbalanced. Machines such as asynchronous motors are manufactured to IEC (International Electrotechnical Commission) standards and voltage unbalance must not exceed 1% at full load [1] or the motor may overheat and burn out. With values of unbalance greater than 1% motors must be de-rated.

Where the load is being powered from a standby generator the situation is worse. Standby generators generally have much higher source impedance, and hence the resulting unbalance figure will be correspondingly higher. Operation on highly unbalance voltage sources, could present serious problems to for other connected load.

In the case of a fine glass furnace other connected load would include essential equipment, such as water cooling circuits, fume extraction fans etc. Failure of this equipment could lead to furnace shut-down, and so the reliability of the whole furnace system is effected.

Three-phase motors are often fitted by unbalance relays to protect them against the effects of an unbalanced voltage supply.

2.2 Limitation of Protection Relays

Motor protection relays generally attempt to simulate the heating effects of an unbalanced voltage on the motor being protected. Their operation is approximate and a margin for error must be included. Many types measure current unbalance at the motor terminals. The negative phase sequence component of the motor current is related to its plugged rotor impedance (which in practice is found to be very close to the locked rotor impedance) and remains nearly constant with load, while the positive phase sequence component varies in accordance with the load. With the increasing percentage of negative phase sequence current at partial load, the motor current becomes more unbalanced. The following calculations demonstrate this point.

Effect of voltage balance on loaded and unloaded motor.

A typical 7.5 kW motor of ABB manufacture is examined and its percentage negative phase sequence current calculated for both the full load and no load conditions. The level of voltage unbalance is taken as 2% negative phase sequence voltage (this being the limit allowed under Quality of Supply Standard EN50160 [2].

The motor is ABB type M2BA 200MLA, 4 pole asynchronous, having a full load rating of 30 kW at 1470 R.P.M. 0.86 power factor, 87% efficiency, 400 volts 50 Hertz.

The motor full load impedance is therefore

$Z_{FL} = 400^2/7500/0.86/1.732/.87 = 16.46\ \Omega$

(magnitude of the star equivalent impedance)

The manufacturer provides values for Z_{NL} (no load) and Z_2 (locked rotor) as follows

$Z_{NL} = 653 + j31.3\ \Omega$

$Z_2 = 1.17 + j2.26\ \Omega$

Therefore $|Z_{NL}| = 653.75\ \Omega$

and $|Z_2| = 2.54\ \Omega$

Examining the full load condition;

Positive phase sequence current (magnitude)

$I_1 = V_1 / Z_{FL}$

$= 230 /16.46$

$= 13.97$ amps

Negative phase sequence current

$I_2 = V_2 / Z$

$= 230 \text{ X } 0.02/2.54$

$= 4.6/2.54$

$= 1.81$ amps

Therefore the percentage negative phase sequence current is given by;

% NPS= 1.81/13.97 %

$= \underline{12.96\ \%}$

Examining the no load condition

Positive phase sequence current (magnitude)

I_1 (no load) = V_1 / Z_t

= 230/653.75

= 0.352 amps

Negative phase sequence current

$I_2 = V_2 / Z_2$

= 230 X 0.02/2.54

= 4.6/2.54

= 1.81 amps

Therefore the percentage negative phase sequence current is given by;

% NPS= 1.81/0.352 %

= 514 %

The purpose of this calculation is to demonstrate the increase in unbalance current as the motor load is decreased. In this case the motor is supplied with 2% unbalance voltage. This represents the maximum limit according to the Quality of Supply Standard EN 50160 [2]. As shown in this example, if the motor is progressively unloaded the percentage negative phase sequence current increases and in the limit reaches 514%.

Many motor protection relays use percentage current unbalance as the trigger for tripping. The tripping level is generally in-built, and set in the region 40% to 80%. It follows that the protection of an unloaded motor is much more problematic. The reliable operation of the unloaded motor is more severely effected by voltage unbalance, if protected by such a relay.

This results in a tendency towards unnecessary and nuisance tripping, because of lower protection reliability at partial load. The consequence for individual motors and hence manufacturing system reliability can be significant where percentage negative phase sequence voltage exceeds 1%.

2.3 Conditions Requiring Balancing

Where large two-phase loads are being installed the owner must study the implications of unbalance from the following perspectives

I. Will equipment be damaged due to the unbalanced voltages?
II. Will the load and other essential equipment operate correctly and reliably given the calculated level of voltage unbalance?
III. Will the resulting voltage unbalanced caused at the point of common coupling to exceed European Supply Quality Standard EN50160 [2]
IV. If a standby generator is installed, will it be capable of supplying the unbalanced load?
V. Will the level of voltage unbalance under standby generator operation, with its different source impedance, be acceptable?

If any one or a number of these conditions is not met, then the user will need to study and implement voltage-balancing techniques to enable proper and reliable operation of the load.

2.4 Harmonic issues

Under European Supply Quality Standard EN50160 [2] limits are set for the maximum voltage unbalance and harmonic distortion which may appear at the point of common coupling between a customer and an electrical utility. The electricity power Regulator will expect network utilities to comply with these limits. Customers are also required not to cause these limits to be exceeded by the operation of their load, and they must take remedial action if they so do.

Even where the 'Quality of Supply' at the point of common coupling is within these limits, that prevailing at load level may be significantly higher, due to circuit impedance. This increase arises from the interaction of the internal distribution system impedances (transformers, cables etc.) and the load.

Electronic load control such as by thyristor, can introduce harmonic distortion and other power quality problems which must be addressed.

The effects of harmonic distortion and thyristor control include the following:

I. Capacitors are susceptible to harmonic overloading. Whilst most are designed to accept 30% over-current, it is the increased stress across the dielectric medium, due to the increased voltage and absorbed harmonic current of the capacitor, which may cause problems. These may exceed the permissible overload conditions allowed in manufacturing specification and design criteria and may lead to early failure. Any capacitors installed where there is known to be harmonic distortion generated, need to be suitably de-rated if the probability of premature failure is to be reduced. Current magnification can also occur and for this further measures are required including the installation of specially designed reactors.

II. The effects on instrumentation control and computers can be a problem. Above a certain level of distortion, some instrumentation and controls are known to produce errors or malfunction, through displacement of zero crossing, or multiple zero crossing superimposed on the voltage waveform. Regulation devices and electronic equipment are subjected to downgraded performance.

III. Induced audio frequency interference may be produced on telephone lines if these run close to power lines and are not suitably screened and segregated.

IV. Higher frequency currents will cause extra heating in cables, switchgear, transformers etc. due to skin effects and hence extra losses in energy and rotating machines; together with additional noise from motors and other apparatus.

V. AC motor and generators can overheat due to the circulation of harmonic currents within the windings. This results from the fact that the negative sequence harmonic voltages (5^{th}, 11^{th} 17^{th} etc.) attempt to rotate the machine in the opposite direction to its normal operation. In this situation these harmonics are attempting to 'plug' the motor. The 'pluging' impedance of an asynchronous machine is found in practice to be very close to the value of its locked rotor impedance. This impedance is in turn generally equal to 1/6 to 1/8 times the value of the loaded impedance. The result is that a significant negative phase sequence current can

flow causing excessive heating of the windings and reducing both the performance and life of the machine.

VI. Thyristor phase angle control introduces a displacement power factor, which can upset current balance if connected across two phases. This is described in chapter 3 of this thesis.

VII. High levels of harmonic distortion can effect the reliability of electrical equipment and any systems of which they form part.

Protection against harmonic distortion is not normally installed on customer equipment; the preferred method being to provide solutions to the harmonic distortion at source, or on the main supply busbar.

2.5 Protection of Standby Generators

In a system that is being powered by a standby generator, the ability of the alternator to supply an unbalanced and harmonically distorted load must also be taken into account. Most standby generator manufacturers include protection so as to prevent damage to alternators arising from excessively unbalanced loads. Generally speaking standby generators will trip when load unbalance exceeds 25%.

Because of the lower short circuit power of a standby generator, an unbalanced load will have a larger effect on voltage balance. This means that where a manufacturing system (including unbalance load) changes from normal supply to a standby generator, its reliability may be substantially reduced. Essential, lightly loaded but critical motors, may trip, resulting in system failure.

Protection against excessive harmonic current and voltage unbalance is not normally installed at the load. The normal solution is to install harmonic filtering at the main switchboard, so as to reduce the level of distortion experienced by the standby generator, and to attempt to rebalance the load.

CHAPTER 3
CONVERTING THREE-PHASE TO TWO-PHASE

3.1 Known Methods

There are a number of known methods of distributing a two-phase load across three phases. These include

- Scott wound transformers
- Capacitor/Inductor Method
- Le Blanc Transformer
- PWM converters
- Motor Generator

The two most commonly used are Scott wound transformers and capacitor-inductor combinations. These two methods are used in the glass industry and are described in the following sections. The remaining methods are discussed briefly for completeness.

3.2 Scott Transformer Method

Scott wound transformers consist generally of two independent two-phase transformers. A centre tap from the primary of the first (main) transformer is brought out and connected to one pole of the primary of the second (called the teaser transformer). The secondaries of these transformers will produce two voltages in quadrature, which can be arranged to be of equal magnitude. Although originally used to supply two-phase motors form a three-phase supply, they can also be arranged to distribute a two-phase load over three phases. This is achieved by leaving the secondary of the main transformer open, and connecting the two-phase load across the secondary of the teaser transformer. The result is that the load current is split in the ratio 2:1:1 across the three-phase supply. The circuit and vector diagrams of this arrangement are shown in Figures 3.1 and 3.2 respectively.

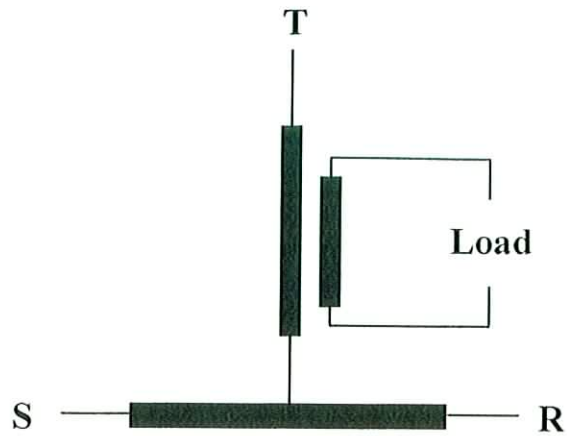


Figure 3.1 Scott transformer circuit diagram

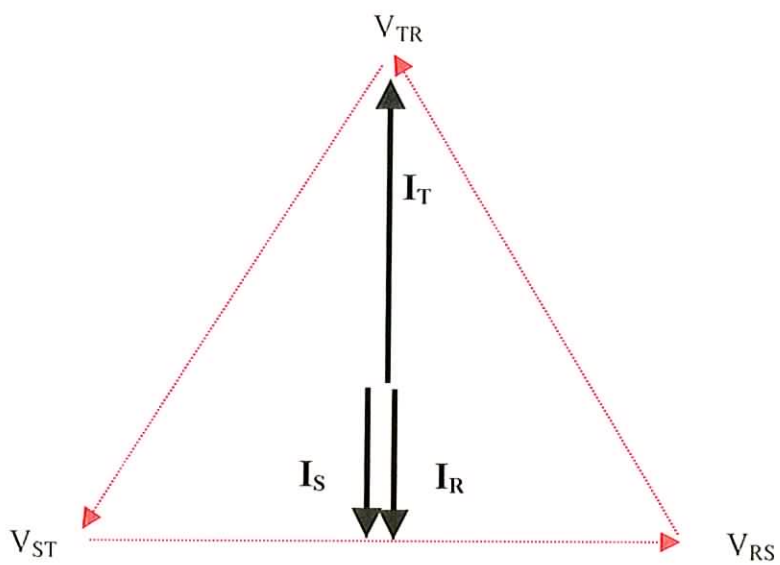


Figure 3.2 Phasor diagram of Scott transformer

V_{RS}, V_{ST} and V_{TR} represent the supply line voltages. I_R, I_S and I_T represent the line currents drawn by the primary of the Scott transformer while supplying a two-phase load.

As can be seen the two-phase current is partially balances across the three phases, however the currents in I_R and I_S are displaced by - 60° and + 60° from the respective

phase voltages. This leads to a high negative phase sequence current component and consequent voltage unbalance.

In practice this type of balancing is improved by adding some two-phase (resistive) load connected across R and S phases, in parallel with the Scott (main) transformer primary. If the amount of this load is appropriately selected and controlled, a perfect current balance can be achieved as shown in the Figure 3.3.

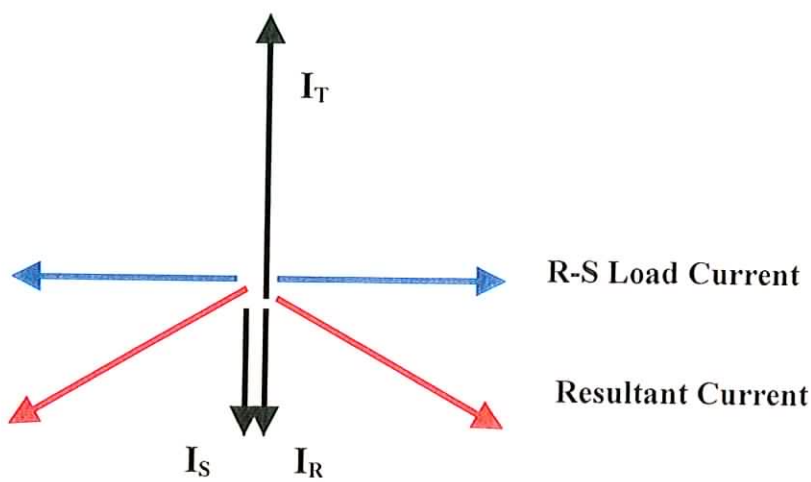


Figure 3.3 Phasor of combined load

The disadvantages of the Scott method are as follows;

I. The Scott transformer method cannot be used alone. Consider Figure 3.4. Additional load must be added to R and S phase to achieve balance. Under varying load conditions, the current ratio between that of the Scott transformer and R-S load must be maintained, otherwise substantial unbalance can arise. Note that this arrangement assumes that the entire load to be balanced is resistive.

II. Difficulties are encountered if the two loads have different power factors. This point is illustrated in Figure 3.4, where the R-S load has a lagging power factor, and the Scott transformer load a unity power factor. In the case of Waterford Crystal the furnace at their Dungarvan plant is arranged so that the Scott transformer supplies variac controlled resistive heater elements. A separate R-S load consists of resistive heating elements controlled by thyristors. These thyristors use phase angle control and so create a displacement power factor and

harmonic currents. As can be seen from Figure 3.4, the resultant currents can be very unbalanced.

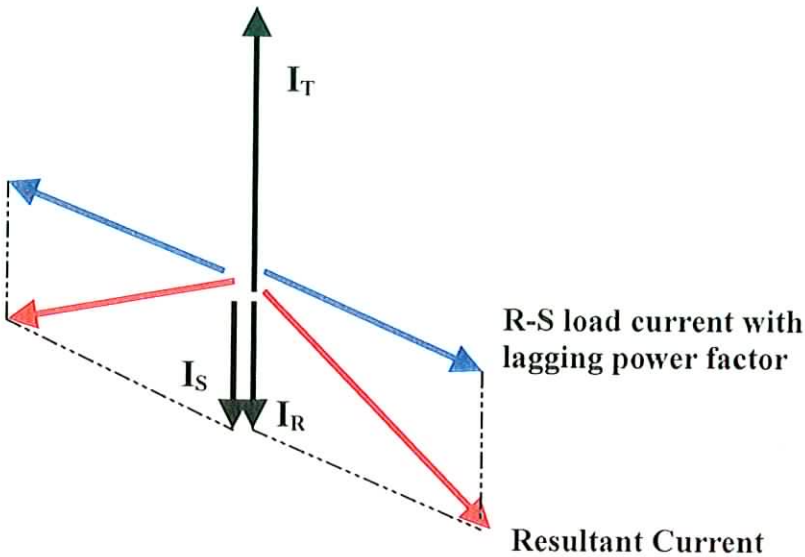


Figure 3.4 Phasor diagram showing effect of lagging power factor

III. Because the thyristor controller effects R and S phases only, an asymmetrical harmonic current will be cause to flow, requiring a specially designed filter system. Figure 3.5 illustrates the situation where the R and S connected load is controlled by two-phase thyristor drives while the Scott transformer load is controlled by means of a voltage regulator.

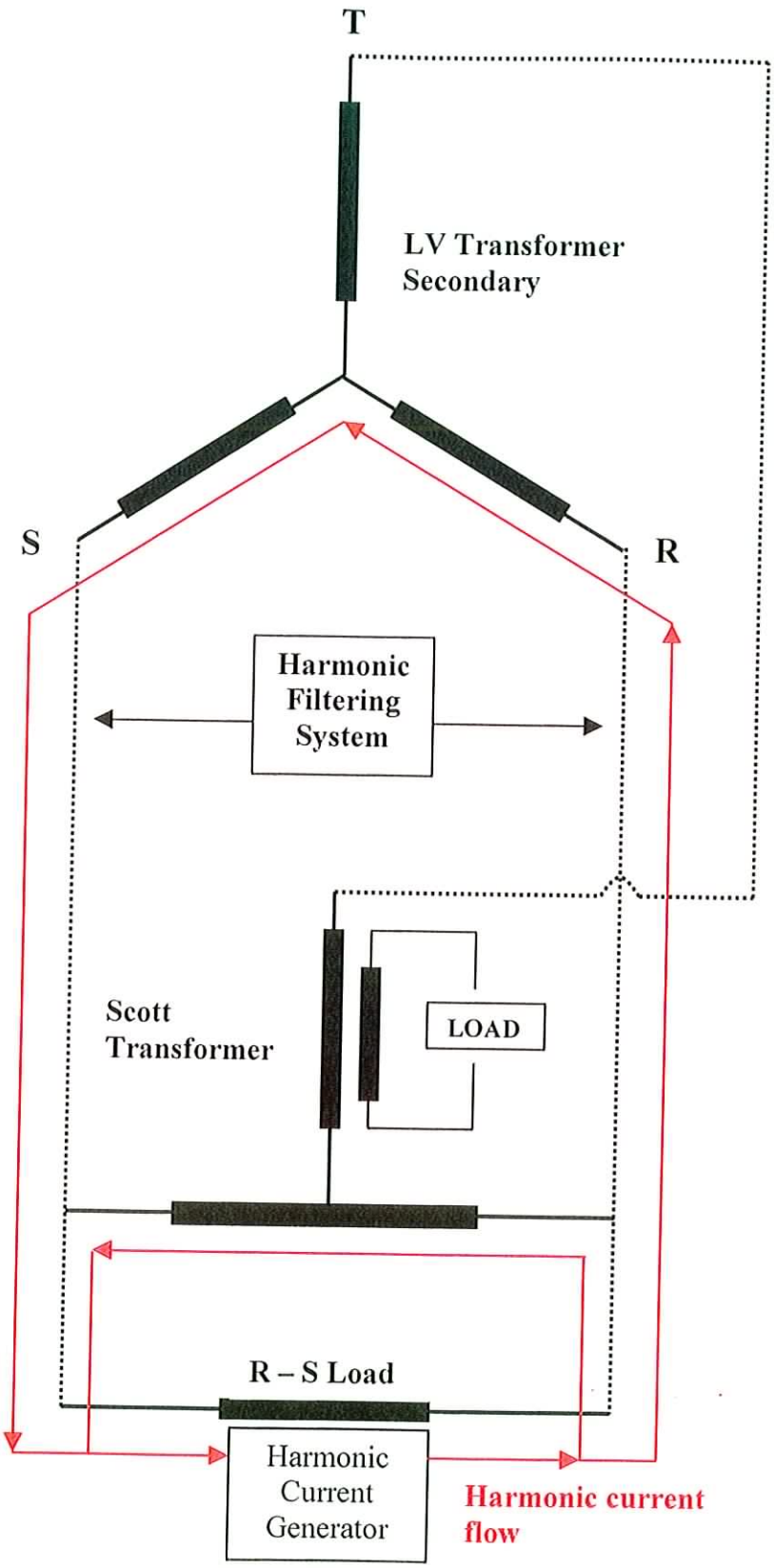


Figure 3.5 Harmonic current flow

IV. The thyristor switching causes odd harmonic currents to be generated. Consider Figure 3.5. This diagram shows a supply transformer star connected secondary, connected to a Scott wound transformer, with a thyristor controlled load supplied across phases R and S. Because this load is single-phase, no triplene cancellation occurs, and all odd harmonics flow. The magnitude of each harmonic current is approximately equal to 1/N times I_{50} where N is the harmonic number and I_{50} is the fundamental current. This means that any filter solution must contain several elements, usually a combination of 3^{rd}, 5^{th} and 7^{th} order filter branches, in order to absorb the harmonic currents of largest value.

V. The Scott transformer is an essential load supply component, and so its failure could have catastrophic consequence. A major disadvantage is that the Scott wound system is non-standard. It requires two high-powered two-phase transformer cores, which have to be of special manufacture. Lead times are very long, and replacement in the event of failure is a critical issue. Being non standard these transformers are expensive to produce. The cost of purchasing and storing a replacement unit therefore becomes an issue.

3.4 Capacitor/Inductor Method

A two-phase resistive load may be converted to three-phase balanced by the connection of an inductor and capacitor between the loaded phases and the unloaded one. The circuit and phasor diagrams Figures 3.6 and 3.7 demonstrate this.

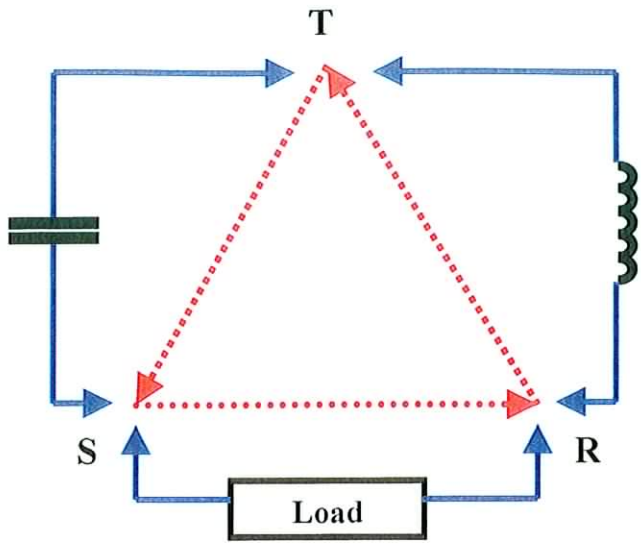


Figure 3.6 Circuit diagram of basic capacitor-inductor balancer

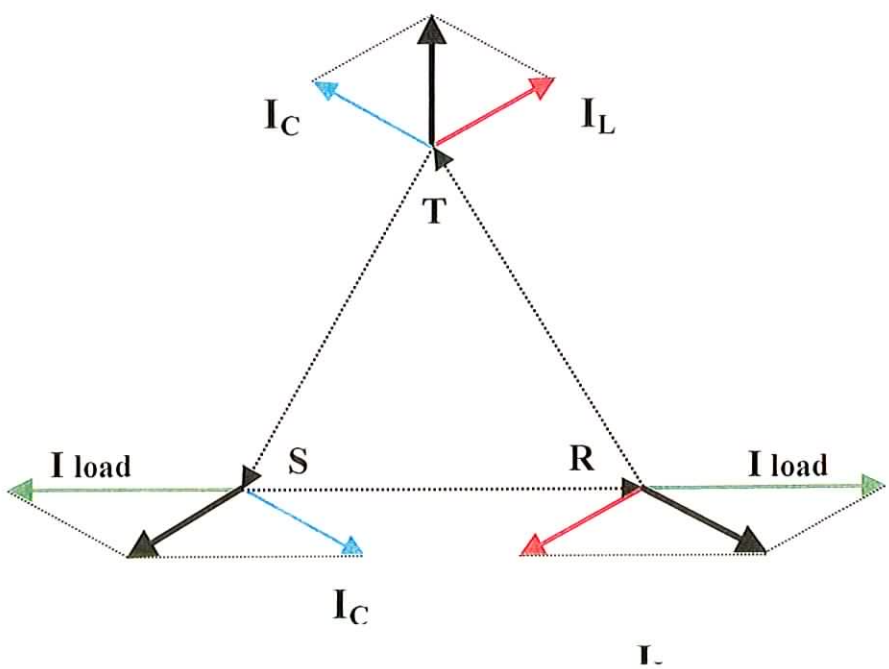


Figure 3.7 Phasor diagram of capacitor-inductor balancer

Figure 3.7 shows the vector diagram for this configuration. $\mathbf{I}_C$ and $\mathbf{I}_L$ represent the capacitor and inductor currents. $\mathbf{I}_{LOAD}$ represents the resistive load current flowing in R and S phases. It can be seen that the appropriate selection of inductor and capacitor values leads to a balanced set of resultant current vectors (shown in black).

To achieve this both I_L and I_C must have the following value:

$$\frac{P}{2V\cos 30} \text{ amps}$$

where P represents the full load power and V the supply system voltage.

Both L and C will in this case have equal reactance at 50 Hz. Note that L and C will form a 50 Hz series tuned circuit across R and S, if T phase is disconnected. Should the T phase become disconnected, this tuned circuit would produce a short circuit between the R and S phases. In practice this situation can arise from fuse failure or loss of phase from the supply source. It can also occur momentarily during the closing or opening of a feeding contactor or circuit-breaker. The latter situation arises due to mechanical time differences in the closing or opening of the individual phase contacts. This can result in violent failure of the capacitor.

3.5 Disadvantage of Capacitor / Inductor Method

The main disadvantage of this method relates to the issues of safety, fire and reliability associated with capacitor failure. This may be caused by centre phase failure, or momentary phase loss due to contact timing differences within connecting devices, leading to momentary but excessive voltage rise on the capacitor.

3.5.1 Voltage rise test

A test was undertaken with production components. A capacitor and a reactor of equal impedance were connected across a 400 volt supply. The capacitor comprised of a series parallel combination with a total continuous voltage withstand of 1,200 volt RMS. Figure 3.8 shows how the circuit was arranged. The reactor was stated by the manufacturer to have a limit of linearity equal to 1.1 times Un (400 V)

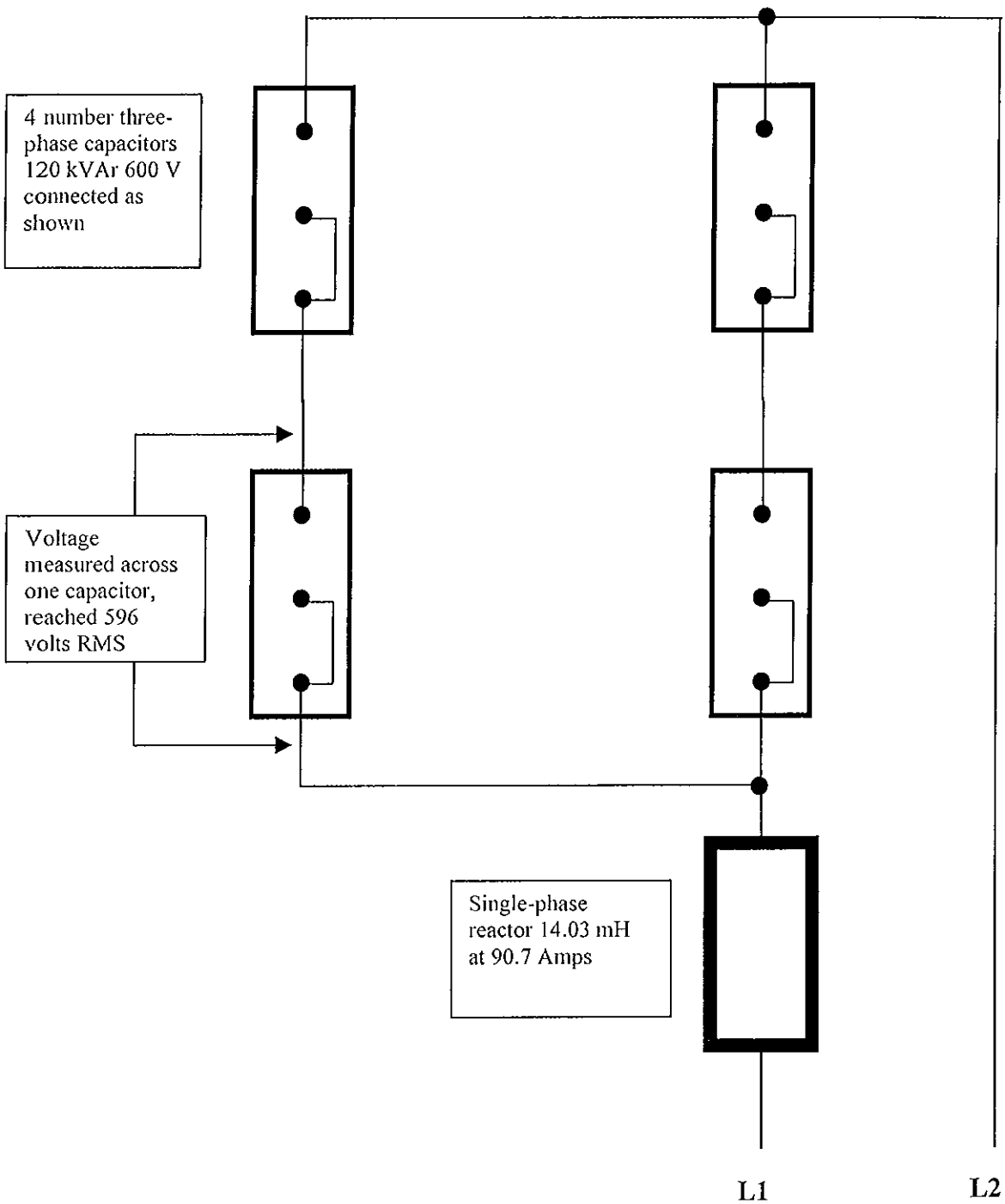


Figure 3.8 Voltage test on production components

This test showed that one capacitor reached a steady state of 596 volts RMS giving an expected value of 1192 volts RMS across a capacitor stage within the balancer.

3.6 Le Blanc Transformer

"The alternative connection to the Scott for transforming three-phase to two-phase is the Le Blanc connection. Although the latter connection has been accepted by engineers from the end of the nineteenth century, it has not gained the same popularity as the Scott connection and is not as well known. In addition the phase displacement obtained by both methods is the same" [3]. This means that the Le Blanc method poses the same problems for furnace manufacturers as the Scott method.

3.6 PWM Converter

Pulse Width Modulated converters are becoming increasingly common in the electrical power industry, due to developments in the manufacture of power transistors. These devices are extensively used in Variable Speed Drives for motors. Based on these units a new type of converter has been developed for the marketplace by a number of leading electrical equipment manufacturers.

These converters operate by rectifying the three-phase supply voltage, storing it in a large DC capacitor, and then inverting the DC using a PWM inverter, to produce a quality controlled AC output. This output is generally three-phase AC, but the unit can easily be programmed to provide a two-phase or single-phase output [4]. Although these units are available, their cost for high power applications is at present 10 to 15 times greater than the method described in this thesis.

3.7 Motor-Generator

A three-phase motor coupled with a single-phase generator can be used for the purpose described in this thesis. In practical terms for furnace loads, the single-phase generator section would be very large, would require special manufacture and would be very expensive to produce. Furnace manufacturers have discounted the use of Motor-Generators on this basis.

CHAPTER 4

A NEW APPROACH TO LOAD PHASE BALANCING

4.1 Introduction

After considering the options available the author decided to design and construct a capacitor/inductor balancer. To overcome the over-voltage problem describes in section 3.5 it was decided to add a permanently connected idling motor in order to limit voltage rise in the event of the centre phase becoming disconnected.

Further investigation indicated that the idling motor could contribute balancing currents if it was supplied from a deliberately unbalanced voltage source. The objective was to reverse the process described by Campbell [5] and make use of inductor motor attributes described by Kemp [6], which could be advantageous in this situation.

The approach described here is based on the addition of suitable three-phase negative sequence currents to that of a two-phase load, in order to create a set of balanced three-phase currents. In order to describe the method it is first necessary to review the work of Kemp [6], and explain its implication for the balancing of unbalanced loads.

4.2 Symmetrical Component Analysis

According to the theory of symmetrical component analysis, any set of three-phase voltages or currents can be represented by the sum of its phase sequence components, positive, negative and zero. For a three-phase system of voltages V_A, V_B and V_C these components are given by the following equations:

Positive phase sequence component $V_1 = (\alpha^2 V_A + \alpha V_B + V_C)/3$

Negative phase sequence component $V_2 = (\alpha V_A + \alpha^2 V_B + V_C)/3$

Zero phase sequence component $V_0 = (V_A + V_B + V_C)/3$

Where α is the 120 degree operator

Similarly for a three-phase system of currents:

Positive phase sequence component $I_1 = (\alpha^2 I_A + \alpha I_B + I_C)/3$

Negative phase sequence component $I_2 = (\alpha I_A + \alpha^2 I_B + I_C)/3$

Zero phase sequence component $I_0 = (I_A + I_B + I_C)/3$

Therefore for any three-phase system of currents

$I = I_1 + I_2 + I_0$

In practice the zero phase sequence component is brought about by the displacement of the three-phase vector group relative to the neutral.
Since both the load and balancer considered in this thesis have no neutral connected, it follows that

I_0 = zero

Therefore $I = I_1 + I_2$

For the remainder of this thesis positive and negative phase sequence components only will be considered.

4.3 Kemp Method

Kemp described a graphical method of deriving the positive and negative phase sequence components of a three-phase system of voltages or currents [5]. The method, outlined here is more suitable for explaining the operation of the balancer.

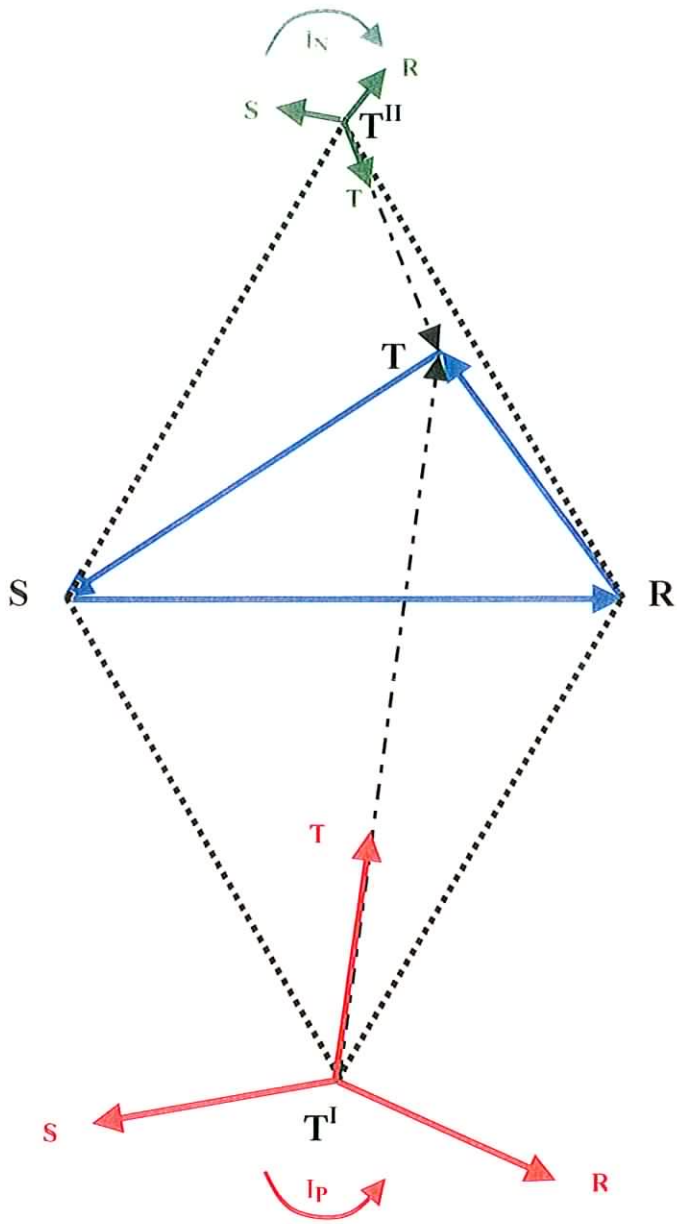


Figure 4.1 Kemp construction for unbalance load

Referring to Figure 4.1; consider a three-phase system of unbalance currents (shown in blue).

Based on the RS phase line, two equilateral triangles are drawn and the extremities marked as T^{I} and T^{II} (shown dotted).

Join T^{I} and T^{II} to T.

Kemp proved the vector $T^{I}\ T \div 3$ represents the magnitude and direction of the T component of a balanced positive phase sequence set of currents (shown in red). The vector $T^{II}\ T \div 3$ represents in magnitude and direction the T component of a balanced negative phase sequence set of currents (shown in green).
As described in section 3.2 $I = I_1 + I_2$

It follows that $I_1 = I - I_2$

From this we can deduce that if a current equal and opposite to the negative phase sequence component, is added to the unbalanced system, the resultant will be a set of balanced positive phase sequence currents.

This argument holds equally well for a two-phase resistive current I_S flowing between two phases (say R and S phases). This current is equivalent to a three-phase system, with I_R flowing in R, I_S ($= - I_R$) flowing in S phase, and zero current flowing in T phase. Figure 4.2 demonstrates, using the Kemp construction, the resolution of this two-phase current into its positive and negative phase sequence three-phase components.

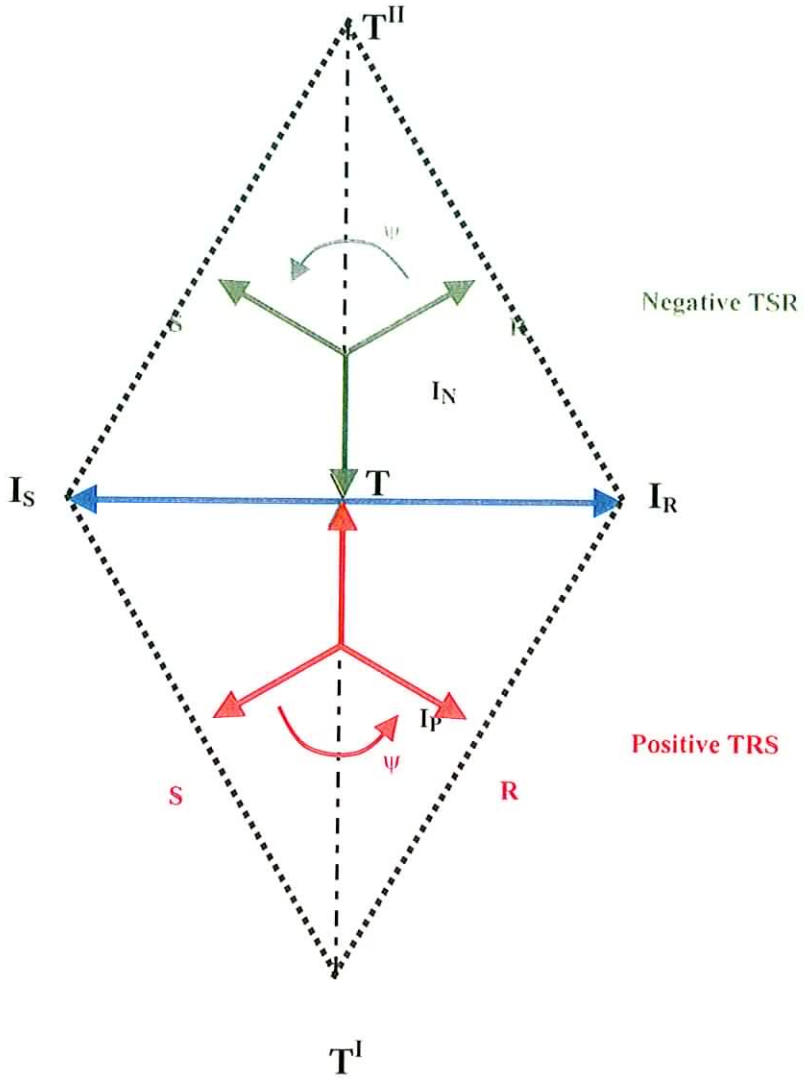


Figure 4.2 Kemp construction for two-phase load

I_S and I_R represent the full load current flowing in R and S phases. If a negative phase sequence current equal and opposite to I_N is injected into the three-phase system, the resultant seen by the supply system is the balanced three-phase positive phase sequence component of I_S and I_R.

4.4 Balancer Description

The balancer described here operates by generating the necessary negative phase sequence currents using an asynchronous motor. This is possible because of the differing negative and positive phase sequence impedances of these machines.

Since the negative phase sequence voltage rotates contrary to the motor rotation, it's associated current is limited only by the plugged rotor impedance, which in practice equals the locked rotor impedance Z_{LR}. The positive phase sequence current is however limited by the load impedance, and this can have a value anywhere between its highest, at no load, and it lowest value, at full load.

Consider an asynchronous motor running at no load. When mains voltage is applied to the motor its impedance is initially equal to its locked rotor value. The ratio of nominal full load impedance Z_{FL} , to starting impedance $Z_{LR,}$ for most asynchronous motors lies in the region 6:1 to 8:1. Furthermore the full load impedance of motors, Z_{FL}, generally equals from 2% to 6% that at no load, Z_{NL}. This means that in practice the ratio of no load to locked rotor impedance, here referred to as N, lies between 100:1 and 400:1, depending on whether the motor is designed for low or high starting torque. It follows that for any unbalanced supply voltage, the motor will draw a much higher current per unit voltage for negative phase sequence voltage component, as for positive phase sequence component.

Take for example ABB motor, catalogue number, M2AA 132M 4 pole 400V 50Hz 7.5 kW.

Manufacturer test data indicates that
No load impedance = $653 + j31.3\ \Omega = |654|\ \Omega$
Locked rotor impedance = $1.17 + 2.26j\ \Omega = |2.55|\ \Omega$

From this $N = 654/2.55 = 256$

Take a supply having a percentage negative phase sequence voltage of 2%;

i.e. $V_2 = 0.02\ V_1$ (where V_1 is the positive phase sequent component and V_2 is the negative phase sequent component)

Then the percentage negative phase sequence current;

$I_2 = 256 \times 2\% \, I_1$

or 5.12 times I_1 (where I_1 is the positive phase sequent component and I_2 is the negative phase sequent component)

If the percentage negative phase sequence voltage is artificially increased to 10% (as will be described later)

i.e. $V_2 = 10\% \, V_2$

then the percentage negative phase sequence current I_2 is

$I_2 = 256 \times 10\% \, I_1$

or 25.6 times I_1

Thus it follows that by deliberately supplying an asynchronous motor with an unbalanced voltage, it is possible to have the motor draw a current, which is largely dominated by its negative phase sequence component. This can be achieved by supplying the motor through an auto-transformer as shown in the Figure 4.3.
(This motor will be referred to as the pilot-motor for the rest of the thesis. The suffix $_p$ as in V_{SP} and V_{RP} will be used for any voltage, current or impedance values referred to this motor)

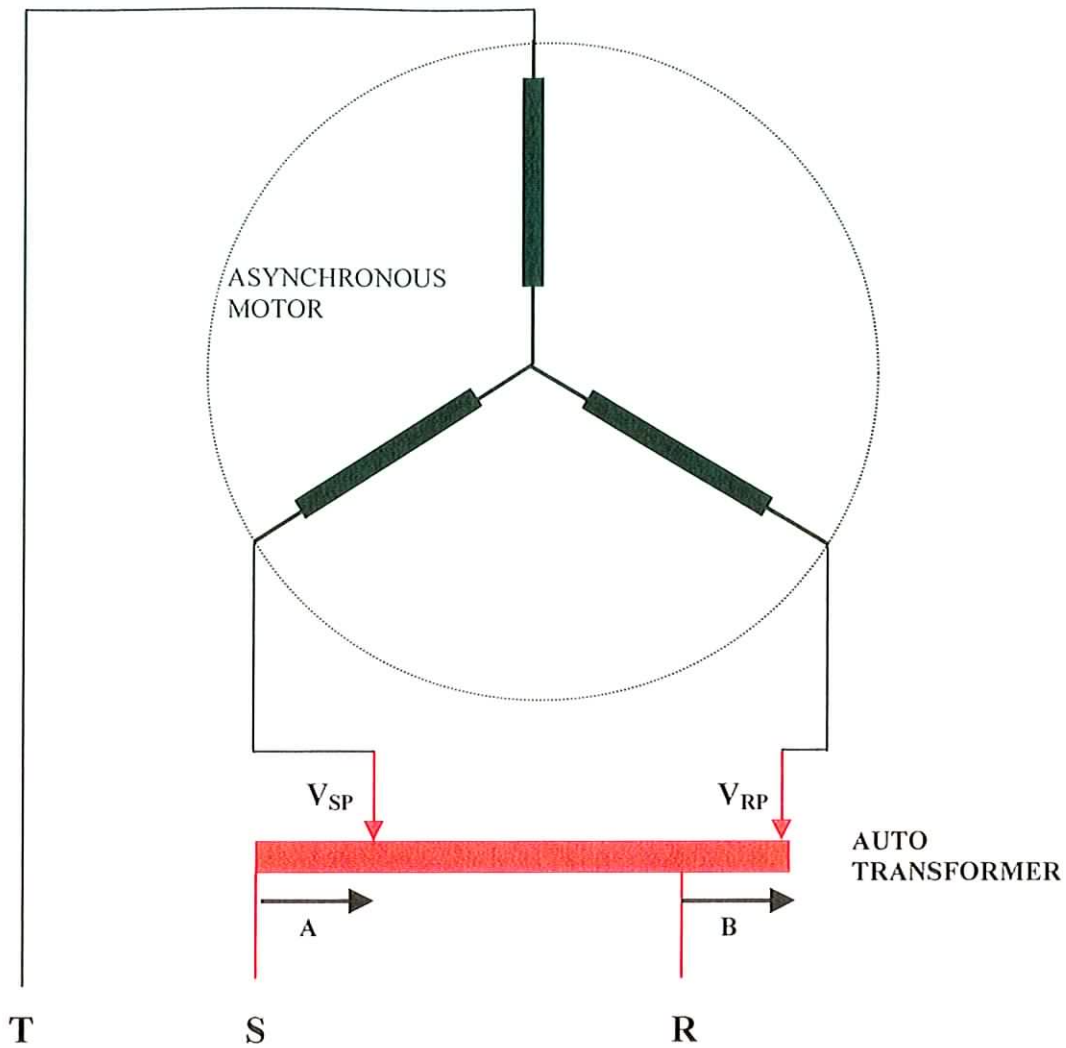


Figure 4.3 Pilot-motor supplied with unbalance voltage from an auto-transformer

The auto-transformer varies the supplied voltage V_{RP} and V_{SP} to the pilot-motor terminals. The voltages are altered by taps A and B near the S and R terminals respectively.
(For calculation purposes within this thesis, values A and B are given in per unit with reference to the auto-transformer input voltage)

By this means the required negative phase sequence current can be generated. By adjustment of taps A and B it is possible to generate a negative phase sequence current equal and opposite to that caused by the two-phase load. By summating the two, a balanced three-phase current is achieved. The balancer must be designed to match the proposed load in order to produce the required current balance, and the method of achieving this will be described in the next chapter.

4.5 Loss Reduction

The losses associated with a pilot-motor balancer are in practice higher than that of a capacitor/inductor model. In order to reduce these losses, part of the load can be balanced by capacitor/inductor stages, and the rest by means of the pilot-motor.

This can be implemented safely, provided the connection point between inductor and capacitor (in this case the T phase) is permanently connected to the motor. Then, if the balancer T phase should now become disconnected from the mains, the motor impedance will prevent the capacitor/inductor combination resonating at 50 Hz, and will act to limit the voltage rise across the capacitor. For the proposed balancer system, the maximum capacitor voltage can be calculated, and the appropriate capacitor selected.

In practice during the development of this thesis, a ratio of 1:1, capacitor/inductor to pilot-motor, has been found give a cost-effective result.

CHAPTER 5

BALANCER DESIGN CALCULATIONS

5.1 Introduction

As discussed in section 4.5 it was decided that a percentage of inductor/capacitor balancing be added to the terminals of the motor balancer. This requires that the T phase be permanently connected between these two systems. All elements, together with the load, can now be inserted. A schematic diagram of the entire system incorporating these elements is shown in Figure 5.1. The balancer can be designed with reference to this schematic diagram. The diagram shows the capacitor/inductor balancing elements together with the load impedance, auto transformer, pilot-motor and the supply system source impedance.

Z_S is the supply source impedance

Z_L is the load impedance

X_L and X_C are the inductor and capacitor balancing elements

A and B are the auto-transformer tap ratios

The suffix $_1$ after a phase letter as in V_{T1} or V_{S1T1} refers to points on the network located on the load side of the system impedance.

The suffix $_P$ as in I_P or V_{1P} denotes values referring to the pilot-motor.

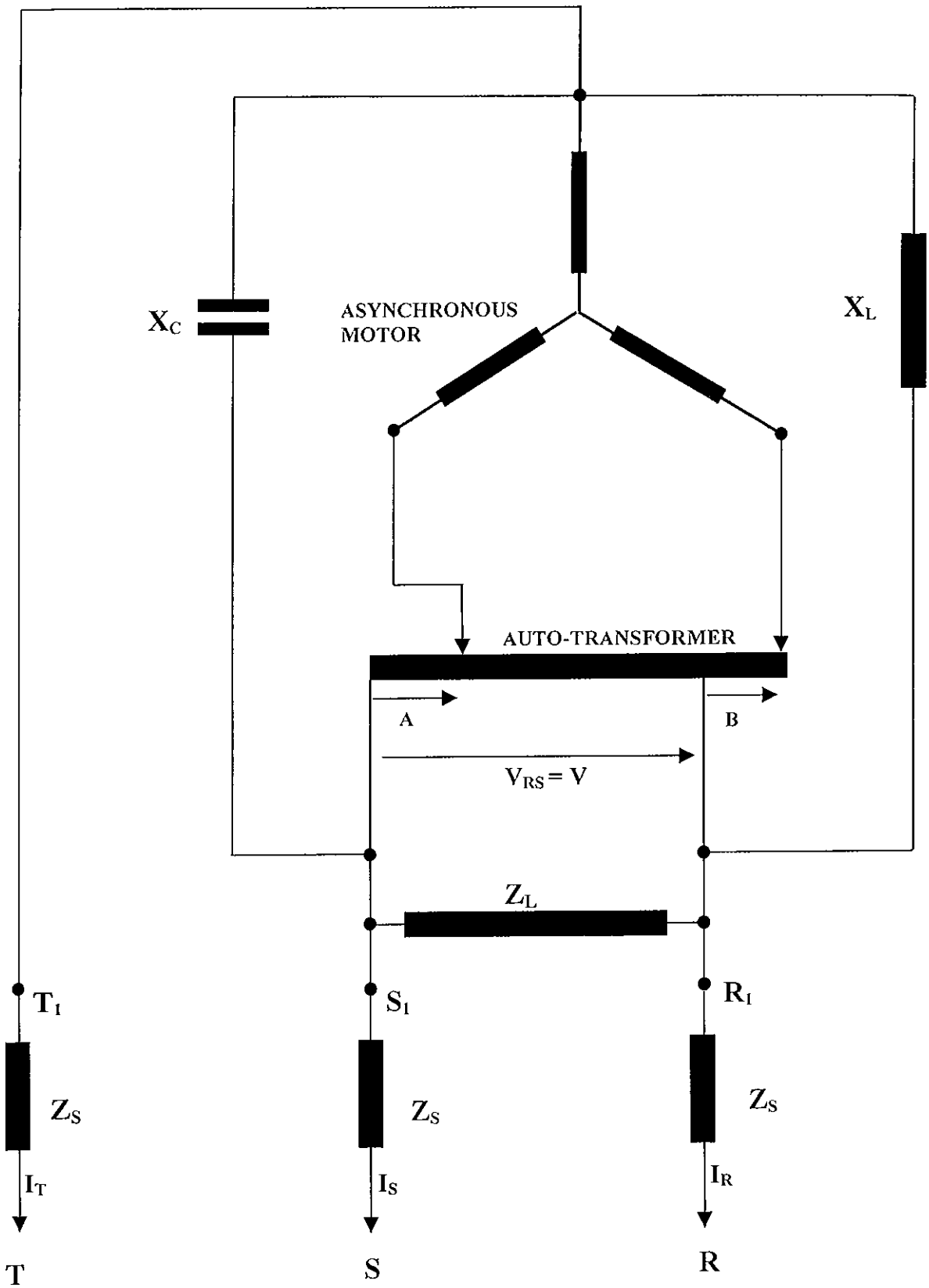


Figure 5.1 Balancer circuit showing source impedance, two-phase load, capacitor-inductor balancer and pilot-motor balancer

5.2 Balancer Calculations

Analysis of this circuit begins with the calculation of the pilot-motor auto-transformer currents, as outlined in Figure 5.2

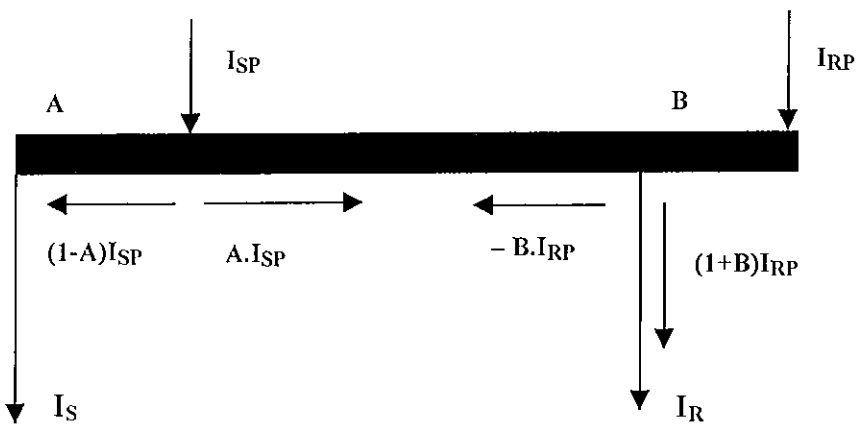


Figure 5.2 Current flow in the auto-transformer

Gathering terms;

$$I_R = (1 + B)I_{RP} + AI_{SP} \quad (1)$$

$$I_S = (1 - A)I_{SP} - BI_{RP} \quad (2)$$

Adding the load Z_L and balancer components X_L and X_C as shown in Figure 11;

$$I_R = (1 + B)I_{RP} + AI_{SP} - V_{TIRI}/X_L + V_{RISI}/Z_L \quad (3)$$

$$I_S = (1 - A)I_{SP} - BI_{RP} + V_{SITI}/X_C - V_{RISI}/Z_L \quad (4)$$

$$I_T = I_{TP} + V_{TIRI}/X_L - V_{SITI}/X_C \quad (5)$$

If the pilot-motor phase currents are taken as I_{RP}, I_{SP} and I_{TP}, then the motor phase sequence components are;

$$I_{RP} = I_{1P} + I_{2P} \quad (6)$$

$$I_{SP} = \alpha^2 I_{1P} + \alpha I_{2P} \quad (7)$$

$$I_{TP} = \alpha I_{1P} + \alpha^2 I_{2P} \quad (8)$$

Figure 5.3 can be used to determine the voltages experienced by the pilot-motor and auto-transformer;

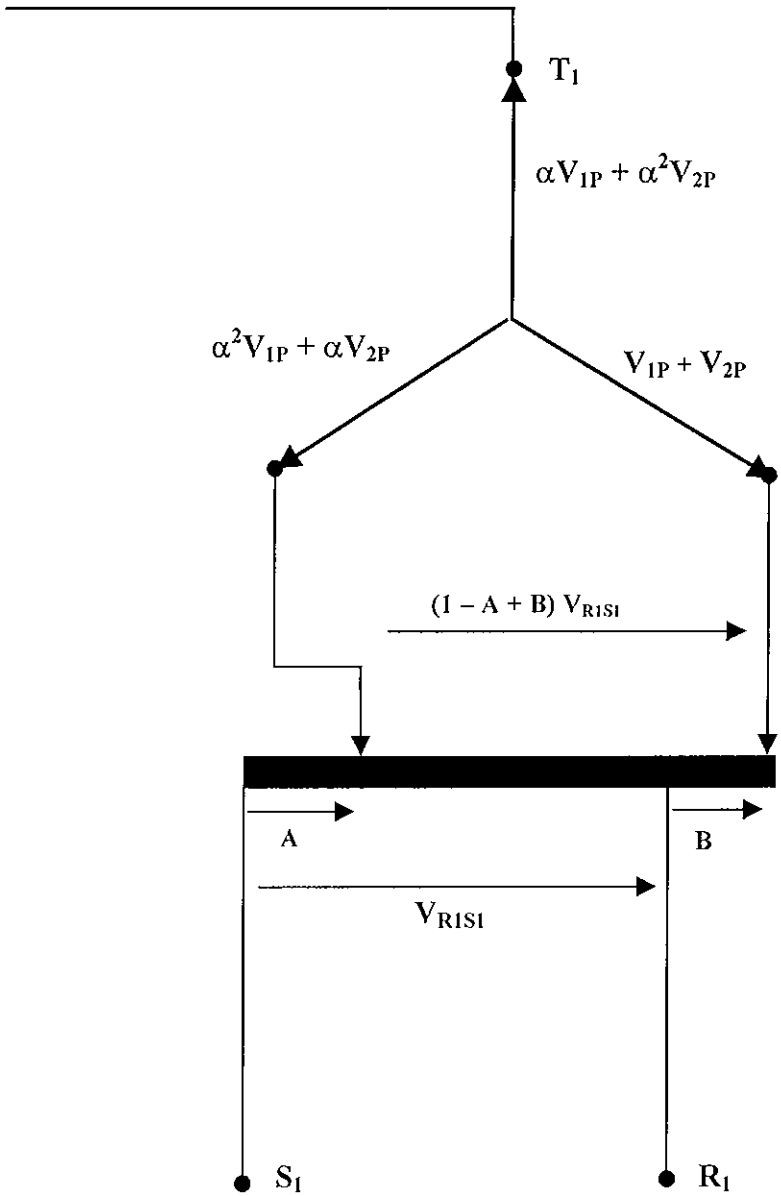


Figure 5.3 Pilot-motor and auto-transformer

Viewing the circuit between terminals R_1 and S_1

$$V_{R1S1} - \{(V_{1P} - V_{2P}) + (\alpha^2 V_{1P} + \alpha V_{2P})\}/(1 - A + B) = 0$$

$$\therefore V_{R1S1} = \{(1 - \alpha^2)/(1 - A + B)\} V_{1P} + \{(1 - \alpha)/(1 - A + B)\} V_{2P} \qquad (9)$$

Viewing the circuit between terminals T_1 and R_1

$$V_{T1R1} + (V_{1P} + V_{2P}) - (\alpha V_{1P} + \alpha^2 V_{2P}) - B V_{R1S1} = 0$$

Substituting equation (9) for V_{R1S1}

$$V_{T1R1} = \{(\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)\}V_{1P} + \{(\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)\}V_{2P} \quad (10)$$

Viewing the circuit between terminals S_1 and T_1

$$V_{S1T1} + (\alpha V_{1P} + \alpha^2 V_{2P}) - (\alpha^2 V_{1P} + \alpha V_{2P}) + AV_{R1S1} = 0$$

Substituting equation (9) for V_{R1S1}

$$V_{S1T1} = \{(\alpha^2 - \alpha) - A(1 - \alpha^2)/(1 - A + B)\}V_{1P} + \{(\alpha - \alpha^2) - A(1 - \alpha)/(1 - A + B)\}V_{2P} \quad (11)$$

Taking equation (3), and substituting the results of equations (6), (7), (9) & (10) for I_{RP}, I_{SP}, V_{R1S1} and V_{T1R1} respectively results in I_R as follows;

$$I_R = (1 + B)(I_{1P} + I_{2P}) + A(\alpha^2 I_{1P} + \alpha I_{2P}) - \{(\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)\}V_{1P}/X_L - \{(\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)\}V_{2P}/X_L + \{(1 - \alpha^2)/(1 - A + B)\}V_{1P}/Z_L + \{(1 - \alpha)/(1 - A + B)\}V_{2P}/Z_L$$

Since $I_{1P} = Y_{1P}.V_{1P}$ and $I_{2P} = Y_{2P}.V_{2P}$ then;

$$I_R = \{(1 + \alpha^2 A + B)Y_{1P} - [(\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)]/X_L + [(1 - \alpha^2)/(1 - A + B)]/Z_L\}V_{1P} + \{(1 + \alpha A + B)Y_{2P} - [(\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)]/X_L + [(1 - \alpha)/(1 - A + B)]/Z_L\}V_{2P} \quad (12)$$

Taking equation (4), and substituting the results of equations (6), (7), (9) & (11) for I_{RP}, I_{SP}, V_{R1S1} and V_{S1T1} respectively results in I_S as follows;

$$I_S = (1 - A)(\alpha^2 I_{1P} + \alpha I_{2P}) - B(I_{1P} + I_{2P}) + \{(\alpha^2 - \alpha) - A(1 - \alpha^2)/(1 - A + B)\}V_{1P}/X_C + \{(\alpha - \alpha^2) - A(1 - \alpha)/(1 - A + B)\}V_{2P}/X_C - \{(1 - \alpha^2)/(1 - A + B)\}V_{1P}/Z_L - \{(1 - \alpha)/(1 - A + B)\}V_{2P}/Z_L$$

Since $I_{1P} = Y_{1P}.V_{1P}$ and $I_{2P} = Y_{2P}.V_{2P}$ then;

$$I_S = \{(\alpha^2 - \alpha^2 A - B)Y_{1P} + [(\alpha^2 - \alpha) - A(1 - \alpha^2)/(1 - A + B)]/X_C - [(1 - \alpha^2)/(1 - A + B)]/Z_L\}V_{1P} + \{(\alpha - \alpha A - B)Y_{2P} + [(\alpha - \alpha^2) - A(1 - \alpha)/(1 - A + B)]/X_C - [(1 - \alpha)/(1 - A + B)]/Z_L\}V_{2P} \quad (13)$$

Taking equation (5), and substituting the results of equations (8), (11) & (10) for I_{TP}, V_{S1T1} and V_{T1R1} respectively results in I_T as follows;

$$I_T = \alpha I_{1P} + \alpha^2 I_{2P} + \{(\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)\}V_{1P}/X_L + \{(\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)\}V_{2P}/X_L - \{(\alpha^2 - \alpha) - A(1 - \alpha^2)/(1 - A + B)\}V_{1P}/X_C - \{(\alpha - \alpha^2) - A(1 - \alpha)/(1 - A + B)\}V_{2P}/X_C$$

Since $I_{1P} = Y_{1P}.V_{1P}$ and $I_{2P} = Y_{2P}.V_{2P}$ then;

$$I_T = \{\alpha Y_{1P} + [(\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)]/X_L - [(\alpha^2 - \alpha) - A(1 - \alpha^2)/(1 - A + B)]/X_C\}V_{1P} + \{\alpha^2 Y_{2P} + [(\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)]/X_L - [(\alpha - \alpha^2) - A(1 - \alpha)/(1 - A + B)]/X_C\}V_{2P} \quad (14)$$

The source voltage is derived from load currents/voltage and system impedance;

$$V_{RS} = (I_R - I_S)Z_S + V_{R1S1} \quad (15)$$

$$V_{TR} = (I_T - I_R)Z_S + (\alpha - 1)V_{1P} + (\alpha^2 - 1)V_{2P} + BV_{R1S1} \quad (16)$$

Taking equations (15), and substituting the results of equations (9), (14), & (12) for V_{R1S1}, I_T and I_R respectively results in V_{RS} as follows;

$$V_{RS} = \{(1 + 2\alpha^2 A - \alpha^2 + 2B)Y_{1P}Z_S - [(\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)]Z_S/X_L - [(\alpha^2 - \alpha) - A(1 - \alpha^2)/(1 - A + B)]Z_S/X_C + 2[(1 - \alpha^2)/(1 - A + B)]\}Z_S/Z_L + (1 - \alpha^2)/(1 - A + B)\}V_{1P} + \{(1 - \alpha + 2\alpha A + 2B)Y_{2P}Z_S - [(\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)]Z_S/X_L - [(\alpha - \alpha^2) - A(1 - \alpha^2)/(1 - A + B)]Z_S/X_C + 2[(1 - \alpha)/(1 - A + B)]\}Z_S/Z_L + (1 - \alpha)/(1 - A + B)\}V_{2P} \quad (17)$$

Taking equations (16), and substituting the results of equations (9), (12), (13), & (14) for V_{R1S1}, I_R, I_S and I_T respectively results in V_{TR} as follows;

$$V_{TR} = \{(\alpha - 1 - \alpha^2 A - B)Y_{1P}Z_S + 2[(\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)]Z_S/X_L$$
$$- [(\alpha^2 - \alpha) - A(1 - \alpha^2)/(1 - A + B)]Z_S/X_C$$
$$- [(1 - \alpha^2)/(1 - A + B)]Z_S/Z_L + B(1 - \alpha^2)/(1 - A + B) + (\alpha - 1)\}V_{1P}$$
$$+ \{(\alpha^2 - 1 - \alpha A - B)Y_{2P}Z_S$$
$$+ 2[(\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)]Z_S/X_L$$
$$- [(\alpha - \alpha^2) - A(1 - \alpha)/(1 - A + B)]Z_S/X_C$$
$$- [(1 - \alpha)/(1 - A + B)]\}Z_S/Z_L + B(1 - \alpha)/(1 - A + B) + (\alpha^2 - 1)\}V_{2P} \quad (18)$$

For ease of computation large sections of equations (17) and (18) are represented by **A1**, **A2**, **A3** and **A4**, as follows;

$$V_{RS} = \mathbf{A1}\ V_{1P} + \mathbf{A2}\ V_{2P} \quad (19)$$

$$V_{TR} = \mathbf{A3}\ V_{1P} + \mathbf{A4}\ V_{2P} \quad (20)$$

where;

$$\mathbf{A1} = (1 + 2\alpha^2 A - \alpha^2 + 2B)Y_{1P}Z_S$$
$$- [(\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)]Z_S/X_L$$
$$- [(\alpha^2 - \alpha) - A(1 - \alpha^2)/(1 - A + B)]Z_S/X_C$$
$$+ 2[(1 - \alpha^2)/(1 - A + B)]\}Z_S/Z_L$$
$$+ (1 - \alpha^2)/(1 - A + B) \quad (21)$$

$$\mathbf{A2} = (1 - \alpha + 2\alpha A + 2B)Y_{2P}Z_S$$
$$- [(\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)]Z_S/X_L$$
$$- [(\alpha - \alpha^2) - A(1 - \alpha^2)/(1 - A + B)]Z_S/X_C$$
$$+ 2[(1 - \alpha)/(1 - A + B)]\}Z_S/Z_L$$
$$+ (1 - \alpha)/(1 - A + B) \quad (22)$$

$$\mathbf{A3} = (\alpha - 1 - \alpha^2 A - B)Y_{1P}Z_S$$
$$- 2[(\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)]Z_S/X_L$$
$$- [(\alpha^2 - \alpha) - A(1 - \alpha^2)/(1 - A + B)]Z_S/X_C$$
$$- [(1 - \alpha^2)/(1 - A + B)]Z_S/Z_L$$
$$+ B(1 - \alpha^2)/(1 - A + B) + (\alpha - 1) \quad (23)$$

$$\mathbf{A4} = (\alpha^2 - 1 - \alpha A - B)Y_{2P}Z_S$$
$$+ 2[(\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)]Z_S/X_L$$
$$- [(\alpha - \alpha^2) - A(1 - \alpha)/(1 - A + B)]Z_S/X_C$$
$$- [(1 - \alpha)/(1 - A + B)]\}Z_S/Z_L$$
$$+ B(1 - \alpha)/(1 - A + B) + (\alpha^2 - 1)\} \quad (24)$$

Resolving (19) and (20) for V_{1P} and V_{2P} gives the positive and negative phase sequence voltage experienced by the pilot-motor are as follows;

$$V_{1P} = (\mathbf{A4}/V_{RS} - \mathbf{A2}/V_{TR})\,(\mathbf{A1}/\mathbf{A4} - \mathbf{A3}/\mathbf{A2}) \quad (25)$$

$$V_{2P} = (V_{RS} - \mathbf{A1}V_{1P})/\,\mathbf{A2} \quad (26)$$

System currents are given as follows where **A1**, **A2**, **A3** & **A4** are as calculated in equations (21), (22), (23) & (24) respectively.

By substituting (25) and (26) into (12), system current I_R can be calculated.

$$\begin{aligned} I_R = {} & \{(1+\alpha^2 A + B)Y_{1P} - [(\alpha - 1) + B(1-\alpha^2)/(1 - A + B)]/X_L \\ & + [(1-\alpha^2)/(1 - A + B)]/Z_L\}\,(\mathbf{A4}/V_{RS} - \mathbf{A2}/V_{TR})\,(\mathbf{A1}/\mathbf{A4} - \mathbf{A3}/\mathbf{A2}) \\ & + \{(1 + \alpha A + B)Y_{2P} - [(\alpha^2 - 1) + B(1-\alpha)/(1 - A + B)]/X_L \\ & + [(1-\alpha)/(1 - A + B)]/Z_L\}\,((V_{RS} - \mathbf{A1}V_{1P})/\mathbf{A2}) \end{aligned} \quad (27)$$

By substituting (25) and (26) into (13), system current I_S can be calculated.

$$\begin{aligned} I_S = {} & \{(\alpha^2 - \alpha^2 A - B).Y_{1P} - [(\alpha^2 - \alpha) - A(1-\alpha^2)/(1 - A + B)]/X_L \\ & - [(1-\alpha^2)/(1 - A + B)]/Z_L\}(\mathbf{A4}/V_{RS} - \mathbf{A2}/V_{TR})(\mathbf{A1}/\mathbf{A4} - \mathbf{A3}/\mathbf{A2}) \\ & + \{(\alpha - \alpha A - B)Y_{2P} + [(\alpha - \alpha^2) - A(1-\alpha)/(1 - A + B)]/X_L \\ & - [(1-\alpha)/(1 - A + B)]/Z_L\}\,((V_{RS} - \mathbf{A1}V_{1P})/\mathbf{A2}) \end{aligned} \quad (28)$$

By substituting (25) and (26) into (14), system current I_T can be calculated.

$$\begin{aligned} I_T = {} & \{\alpha Y_{1P} + [(\alpha - 1) + B(1-\alpha^2)/(1 - A + B)]/X_L \\ & - [(\alpha^2 - \alpha) - A(1-\alpha^2)/(1 - A + B)]/X_C\}\,(\mathbf{A4}/V_{RS} - \mathbf{A2}/V_{TR})\,(\mathbf{A1}/\mathbf{A4} - \mathbf{A3}/\mathbf{A2}) \\ & + \{\alpha^2 Y_{2P} + [(\alpha^2 - 1) + B(1-\alpha)/(1 - A + B)]/X_L \\ & - [(\alpha - \alpha^2) - A(1-\alpha)/(1 - A + B)]/X_C\}\,((V_{RS} - \mathbf{A1}V_{1P})/\mathbf{A2}) \end{aligned} \quad (29)$$

Balancer and load terminal voltages can be calculated as follows;

$$V_{R1S1} = V_{RS} + Z_S(I_S - I_R) \quad (30)$$

$$V_{S1T1} = V_{ST} + Z_S(I_T - I_S) \quad (31)$$

$$V_{T1R1} = V_{TR} + Z_S(I_R - I_T) \quad (32)$$

Balancer and load terminal voltages can be resolved into their phase sequence components as follows;

$$V_{11} = (V_{T1R1} - \alpha^2 V_{R1S1})/3/\alpha \quad (33)$$

$$V_{21} = (V_{T1R1} - \alpha\, V_{R1S1})/3/\alpha \quad (34)$$

Percentage negative phase sequence voltage arising from any combination of A tap and B tap on the auto-transformer can be calculated as follows;

Percentage negative phase sequence voltage at the system terminals is given by;

$$\%V_{NPS} = 100(V_{21}/V_{11}) \quad (35)$$

The following observations are also drawn from the above analysis;

The pilot-motor current, phase sequence components are given by;

$$I_{1P} = Y_{1P} \times V_{1P} \quad (36)$$

$$I_{2P} = Y_{2P} \times V_{2P} \quad (37)$$

From this the pilot-motor phase currents can be calculated as follows;

$$I_{RP} = I_{1P} + I_{2P} \quad (38)$$

$$I_{SP} = \alpha^2 I_{1P} + \alpha I_{2P} \quad (39)$$

$$I_{SP} = \alpha I_{1P} + \alpha^2 I_{2P} \quad (40)$$

The auto-transformer current and kVA ratings per section are calculated as follows;

Section 'A' current = $(1 - A)I_{SP} - B.I_{RP}$	(41)
Section 'A' kVA = $A\{(1 - A)I_{SP} - BI_{RP}\}$	(42)
Mid section current = $AI_{SP} + BI_{RP}$	(43)
Mid section kVA = $(1 - AV)(AI_{SP} + BI_{RP})$	(44)
Section 'B' current = I_{RP}	(45)
Section 'B' kVA = BI_{RP}	(46)

5.3 Calculation of Centre Phase Voltage

Should the centre phase (T in this case) become disconnected from the balancing system, it is important to know the voltage to which the capacitor and inductor will be subjected.

This calculation is similar to that in section 5.1 except that Z_S is taken as zero. This assumption produces a marginally higher capacitor voltage requirement, thus erring on the safe side, while simplifying the calculation process.

Replacing the balancer terminal voltages (subscript 1) in equations (3), (4) and (5) with the supply source voltages gives;

$$I_R = (1 + B)I_{RP} + AI_{SP} - V_{TR}/X_L + V_{RS}/Z_L \quad (47)$$

$$I_S = (1 - A)I_{SP} - BI_{RP} + V_{ST}/X_C - V_{RS}/Z_L \quad (48)$$

$$I_T = I_{TP} + V_{TR}/X_L - V_{ST}/X_C = 0 \quad (49)$$

Note in this case $I_T = 0$

Replacing the balancer terminal voltages (subscript 1) in equations (9), (10) and (11) with the supply source voltages gives;

$$V_{RS} = \{(1 - \alpha^2)/(1 - A + B)\}V_{1P} + \{(1 - \alpha)/(1 - A + B)\}V_{2P} \quad (50)$$

$$V_{TR} = \{(\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)\}V_{1P} + \{(\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)\}V_{2P} \quad (51)$$

$$V_{ST} = \{(\alpha^2 - \alpha) - A(1 - \alpha^2)/(1 - A + B)\}V_{1P} + \{(\alpha - \alpha^2) - A(1 - \alpha)/(1 - A + B)\}V_{2P} \quad (52)$$

For ease of computation let

$\mathbf{B1} = (1 - \alpha^2)/(1 - A + B)$

$\mathbf{B2} = (1 - \alpha)/(1 - A + B)$

$\mathbf{B3} = (\alpha - 1) + B(1 - \alpha^2)/(1 - A + B)$

$\mathbf{B4} = (\alpha^2 - 1) + B(1 - \alpha)/(1 - A + B)$

$$\therefore \quad V_{RS} = \mathbf{B1}V_{1P} + \mathbf{B2}V_{2P} \tag{53}$$

$$\text{and} \quad V_{TR} = \mathbf{B3}V_{1P} + \mathbf{B4}V_{2P} \tag{54}$$

From equation (49);

$$I_{TP} = V_{ST}/X_C - V_{TR}/X_L \tag{55}$$

Combining equations (55) and (8);

$$\alpha I_{1P} + \alpha^2 I_{2P} = V_{ST}/X_C - V_{TR}/X_L$$

$$\therefore \quad \alpha Y_{1P}.V_{1P} + \alpha^2 Y_{2P}V_{2P} = V_{ST}/X_C - V_{TR}/X_L \tag{56}$$

Since $V_{ST} = -V_{RS} - V_{TR}$

$$\therefore \quad \alpha Y_{1P}V_{1P} + \alpha^2 Y_{2P}V_{2P} = (-V_{RS} - V_{TR})/X_C - V_{TR}/X_L \tag{57}$$

Combining equations (57) and (54);

$$\alpha Y_{1P}V_{1P} + \alpha^2 Y_{2P}V_{2P} = \{-V_{RS} - (\mathbf{B3}V_{1P} + \mathbf{B4}V_{2P})\}/X_C - (\mathbf{B3}V_{1P} + \mathbf{B4}V_{2P})/X_L$$

$$\therefore \quad \alpha Y_{1P}V_{1P} + \alpha^2 Y_{2P}V_{2P} = (-V_{RS} - \mathbf{B3}.V_{1P} - \mathbf{B4}V_{2P})/X_C - (\mathbf{B3}V_{1P} + \mathbf{B4}V_{2P})/X_L \tag{58}$$

From equation (53);

$$V_{2P} = (V_{RS} - \mathbf{B1}V_{1P})/\mathbf{B2} \tag{59}$$

Combining equations (58) and (59);

$$\alpha Y_{1P}V_{1P} + \alpha^2 Y_{2P}[\,(V_{RS} - \mathbf{B1}V_{1P})/\mathbf{B2}] =$$

$$(-V_{RS} - \mathbf{B3}V_{1P} - \mathbf{B4}[\,(V_{RS} - \mathbf{B1}V_{1P})/\mathbf{B2}])/X_C$$

$$-\ (\mathbf{B3}V_{1P} + \mathbf{B4}[\,(V_{RS} - \mathbf{B1}V_{1P})/\mathbf{B2}]\,)/X_L$$

$$\therefore \quad \{\alpha Y_{1P} + \alpha^2 Y_{2P}\mathbf{B1}/\mathbf{B2} + \mathbf{B3}/X_C$$

$$-\mathbf{B1B4}/(\mathbf{B2}X_C) + \mathbf{B3}/X_L - \mathbf{B1B4}/(\mathbf{B2}X_L)\}V_{1P}$$

$$= \{-\alpha^2 Y_{2P}/\mathbf{B2} - 1/X_C - \mathbf{B4}/(\mathbf{B2}X_C) - \mathbf{B4}/(\mathbf{B2}X_L)\}V_{RS}$$

$$\therefore \quad V_{1P} = \{-\alpha^2 Y_{2P}/\mathbf{B2} - (1+\mathbf{B4}/\mathbf{B2})\,1/X_C - (\mathbf{B4}/\mathbf{B2})1/X_L)\}$$

$$/\{\alpha Y_{1P} + \alpha^2 Y_{2P}\mathbf{B1}/\mathbf{B2} + (\mathbf{B3} - \mathbf{B1}/\mathbf{B2})1/X_C)$$

$$+ (\mathbf{B3} - \mathbf{B1B4}/\mathbf{B2})1/X_L)\}V_{RS} \qquad (60)$$

From equation (53);

$$V_{2P} = (V_{RS} - \mathbf{B1}V_{1P})/\mathbf{B2} \qquad (61)$$

Capacitor and inductor voltages, with the centre phase (T) removed are as follows using equations (54) and (56);

$$V_{TR} = \mathbf{B3}V_{1P} + \mathbf{B4}V_{2P} \qquad (62)$$

$$V_{ST} = -V_{RS} - V_{TR} \qquad (63)$$

5.4 Balancer Programme

Altering the values of the auto-transformer tappings can now modify percentage negative phase sequence voltage at the load terminals. There exists optimum transformer tappings, which will give the lowest negative phase sequence value. This may be calculated using the iterative process outlined in the balancer programme flow diagram, Figure 5.4.

This iterative programme calculates the percentage voltage negative phase sequence arising form a range of combinations of A tap and B tap on the auto-transformer. The programme is given a wide range of A and B and an incremental step value.

The relevant voltage and impedances are entered. The programme iterates through all combinations of A and B and memorises the settings which give the lowest value. The programme then outputs all calculated values for the optimum settings, which are necessary to design the balancer.

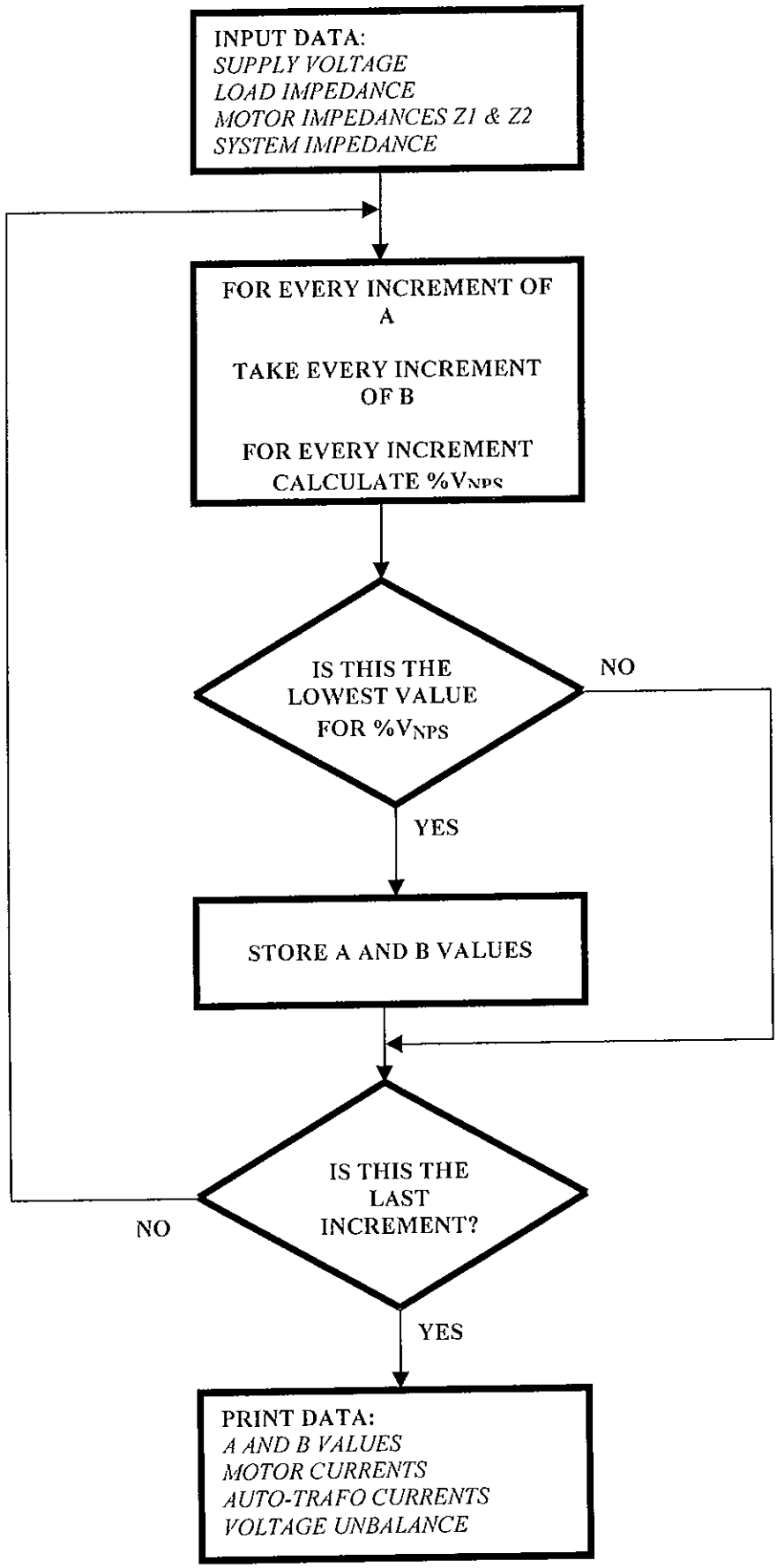


Figure 5.4 Balancer Programme Flow Diagram

This flow diagram was used as the basis for a programme, written in Borland C^{++} which calculates the auto-transformer tapping points and component parameters necessary for the full design, see appendix A.

The layout begins by making all necessary declarations.
This is follower by calculation subroutines, which contain the formulae derived in this chapter. These are followed by the 'find best AB subroutine'.
This is in turn followed by the main programme, which contains data entry and checking.

The programme is compiled to and executable file, which runs under a DOS environment and prints its output to screen. The output can be copied and pasted to MS Word.

A typical programme output is shown in Table 5.1.

```
System voltage  = 400
Load terminal voltage =  397.174
XL = (0, 1.6)
XC = (0, - 1.6)
Motor Z1 'ohms' = (0.066, 1.83)
Motor Z2 'ohms' = (.031, 0.15)
System impedance (ohms) = (0.00139, 0.00733)
Load impedance (ohms) = (0.53333, -0)

A = 0.225,    B = 0.155
Pilot-motor amps, Ir = 272.749,   Is = 63.9755,   It = 234.632
Load and balancer total IR amps = 458.609,  at power factor  0.950579
Load and balancer total IS amps = 460.204,  at power factor  0.950337
Load and balancer total IT amps = 459.1,  at power factor  0.949519
Negative phase sequence voltage % =  0.00306933

Auto-transformer current AV section  = 49.581
Auto-transformer KVA in AV section = 11.1557
Auto-transformer current mid section = 56.6706
Auto-transformer KVA in middle section = 43.9197
Auto-transformer current BV section = 272.749
Auto-transformer KVA in BV section = 42.2761

Capacitor voltage with T phase removed = 473.603
Inductor voltage with T phase removed = 295.324
```

Table 5.1 Balancer programme output

CHAPTER 6

SYSTEM DESIGN & CONSTRUCTION

This chapter outlines the general approach to balancer system design and includes a description of the construction and testing of a prototype unit, together with the design and operation of the first full scale working model.

6.1 Design procedure

Following the calculation stage the process of designing the balancer system consists of integrating the following stages to arrive at the complete solution;

- capacitor/inductor component selection
- pilot-motor selection
- auto-transformer design
- balancer protection design
- balancer control design

6.1.1 Capacitor / Inductor Dimensioning

As discussed in section 4.4 the capacitor/inductor components are calculated to provide balance for 50% of this total load current. The current to be carried by the inductors and capacitors $\mathbf{I_L}$ and $\mathbf{I_C}$ is calculated as follows:

I_L and $I_C = I_{LOAD}/4$

where I_{LOAD} represents the total two-phase load to be balanced

From this $C = I_C/\omega V$

and $L = V/\omega I_L$

6.1.2 Motor Selection

In order to select a suitable pilot-motor an estimate of the required motor current rating is first calculated. This is achieved by calculation the equivalent three-phase current corresponding to the remaining unbalanced two-phase load. The calculation is as follows;

$$I_{MOTOR} = I_{LOAD} / \sqrt{3}$$

This provides an initial estimate of the required current rating of a suitable pilot-motor.

A pilot-motor is selected bearing in mind the following criteria.

I. Current required. That is the magnitude of negative phase sequence current required for balance.
II. Motor loss. A low loss motor should be selected since this motor will run continuously.
III. Current ratio, starting to full load (I_S/I_N). This should be high to give a high negative to positive phase sequence current ratio.

Test results for locked rotor and no load impedances must be obtained from the manufacturer, else they must be measured. Using the balancer programme [appendix A], the pilot-motor loading is calculated. If necessary a different motor should be selected and the process repeated until the most economic result is achieved.

6.1.3 Auto-transformer

An auto-transformer is specified and constructed, or else purchased. This should have voltage tappings A and B as shown in Figure 4.2. The current and kVA ratings should be as calculated by the balancer programme.
Extra tappings near A and B should be included for final adjustment.

6.1.4 T phase connection

Connection of T phase must be maintained between the pilot-motor and the Capacitor / inductor steps. This will prevent the capacitors from being subjected to over-voltage, as already referred to in section 4.2.

6.1.5 Balancer Protection

Both short circuit and overload protection should be provided for the balancer. For the capacitor/inductor elements, miniature circuit breakers are recommended because of their close excess-current protection. The pilot-motor should be protected by a separate moulded case circuit breaker. This will provide short circuit and coarse excessive current protection. Accurate overload protection for the pilot-motor can be provided by means of winding imbedded thermistors. Standard motor protection relays will provide false tripping due to the high level of negative phase sequence current.

6.1.6 Balancer Control

The balancer is adjusted for load variation by means of the capacitor/inductor elements. This section is divided into a number of steps. Step size should be calculated to provide adjustment of V_{NPS} within the desired limits. Load current is sensed by current relays and capacitor/inductor steps are switched accordingly.

6.2 The Prototype Unit

6.2.1 Purpose of Prototype

A prototype unit was built to balance a test furnace. This was installed on a trial furnace located at the Waterford Crystal factory in Butlerstown, Dungarvan. This furnace had a two-phase heating load of 30kW, connected across two phases of a 400 volt three-phase supply.

The objective was to demonstrate the satisfactory operation of the balancer to the client. A decision on the future use of this system with a full-scale production furnace depended upon the outcome of this test.

6.2.2 Component Selection

The prototype unit consisted of two pilot-motors and five capacitor/inductor steps.

The capacitors used were:-

Three-phase 5 kVAr 400 volt units (with two connections only, being used).

This gives a two-phase rating of 2.5 kVAr at 400 volts with $X_C = 64\ \Omega$ and $C = 50\ \mu F$

The inductors were also rated at 64 Ω, giving L = 203.7 mH

The pilot-motors used were ABB catalogue number M2AA 132M, 4 pole, 400 Volt, 50 Hz, 7.5 kW. For these motors manufacturers date indicated;

- $Z_1 = 653 + j31.3\ \Omega$
- $Z_2 = 1.17 + j2.26\ \Omega$
- Current rating is 14.8 amps at 0.83 power factor.

Z1 and Z2 are the positive and negative phase sequence impedances of the motor running under no-load. The motor manufacturer provided this data.

6.2.3 Design Calculations

Running the balancer programme software gave optimum values for

A = 0.2125 V and B = 0.0975 V

The maximum pilot-motor current was calculated at 9.98 amps.

Maximum capacitor voltage with T phase removes was calculated at 488 volts (neglecting motor saturation effects).

The auto-transformer ratings for each section were calculated at

- A section -- 7.51 amps, 1.59 kVA
- Centre section -- 2.95 amps, 2.32 kVA
- B section -- 9.45 amps, 0.921 kVA

Two auto-transformers were constructed as shown in Figure 6.1. The core and winding layout can be seen at the top of this diagram. The drawing also shows the main tappings and additional taps brought out to terminal. The purpose of these was to allow for fine tuning during the commissioning and testing phase.

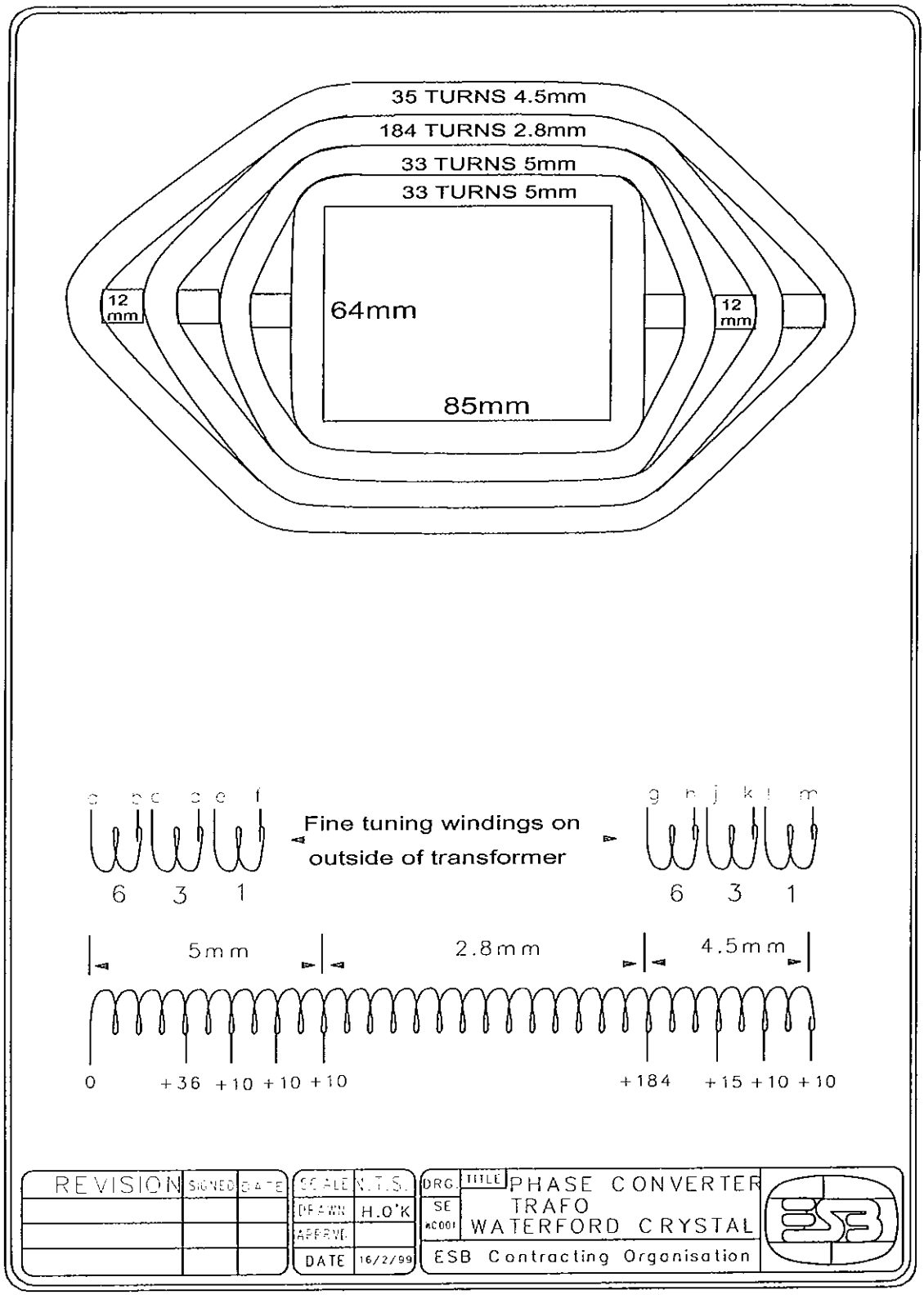


Figure 6.1 Auto-transformer construction

The balancer was then connected as shown in Figure 6.2. This drawing shows the connection of the two motors and of the capacitors and inductors. The connection of the protection relays is also shown.

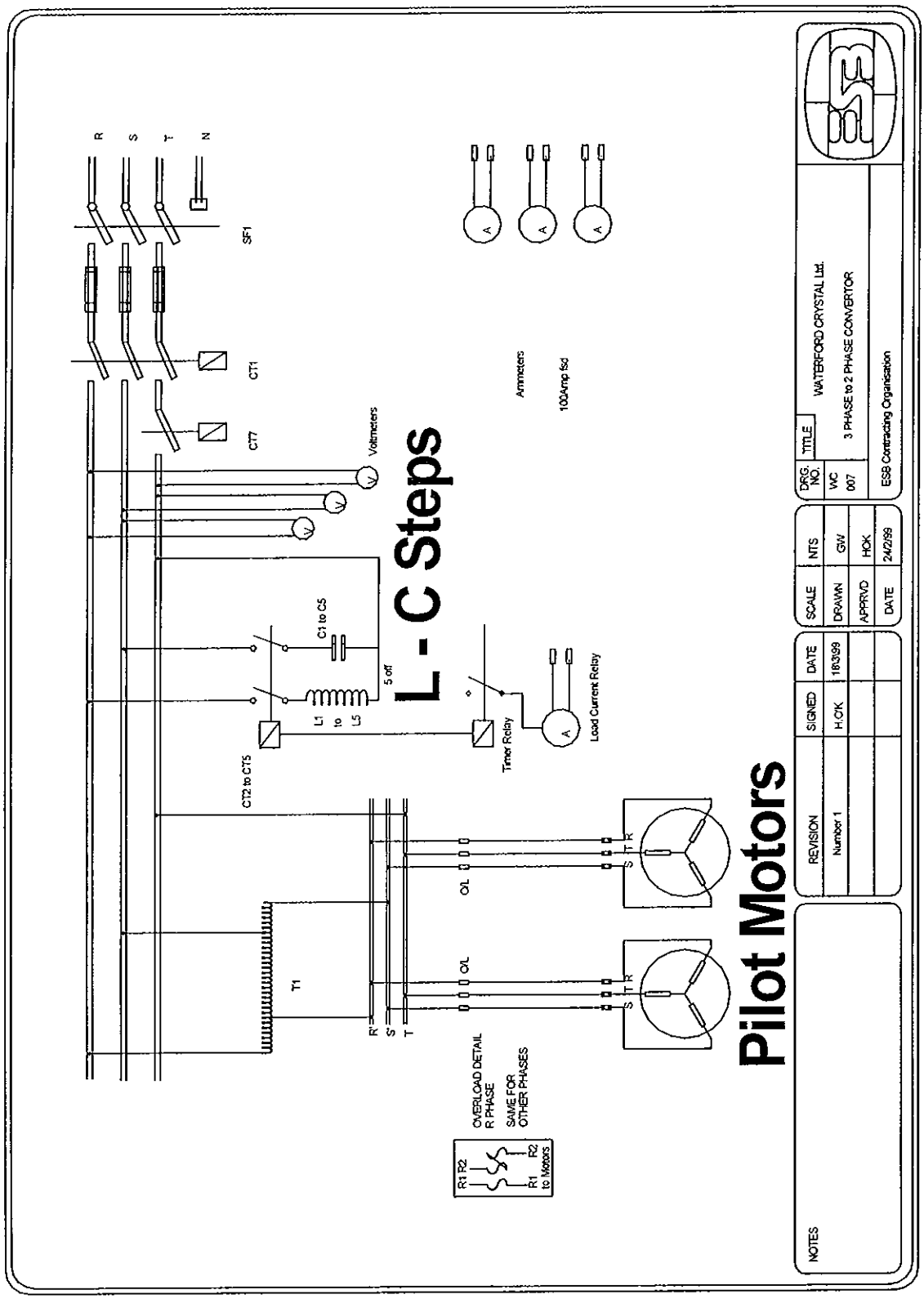


Figure 6.2 Schematic drawing of test balancer

6.2.4 Construction

Appendix C shows in photographic detail the construction of the prototype unit. This unit was supplied in a single housing. The motors were located at either end of the bottom section, with the auto-transformer and capacitor/inductor section between. The top section houses the control circuitry and switching components. Within this section the capacitor/inductor step controls can be seen on the left. A special contactor (middle right) allows the T phase to be disconnected for test purposes. A switch was installed on the front panel for this purpose.

6.2.5 Testing

Tests results for the final assembly are shown in the current vector diagram, appendix D. This drawing shows to scale, the measured results for load and balancer. Measurements were taken using a Dranetz PP1 power quality analyser. This instrument can display voltage and current values and their relative polar displacements.

The phase to neutral voltages are displayed in yellow. The two-phase load current vectors I_R and I_S are displayed in red. The injected balancer currents are displayed in blue. It can be seen from the measurements, that the combination of these two vector groups produced a balance three-phase set of currents, resultant I_R and I_S are shown in light blue and injected I_T in dark blue. The resultant currents are:

I_R = 20.02 amps

I_S = 20.01 amps

I_T = 19.97 amps

The power factor was 0.83

T phase was then removed by switching the specially installed contactor. The resulting voltages across capacitor and inductor, with reference to a 400 volt supply, were as follows:

Capacitor voltage V_{ST} = 440 volts

Inductor voltage V_{TR} = 380 volts

The difference between these and the calculated values can be explained by the saturation of the motor iron core at higher voltage. This has the effect of reducing the voltage experienced by the capacitor.

6.3 The Full Scale Production Model

6.3.1 Introduction

Following the successful operation of the test balancer, a full-scale model of the phase balancer was subsequently constructed and installed at the Waterford Crystal plant, Kilbarry, Waterford City. This unit was connected to the low voltage distribution board supplying the furnace. The furnace consists of two main sections. The first is the Tank, where the solid glass filings are heated to a molten state. The second is a long section of furnace called the Forehearth. From this section glass blowers, and robotic production machinery, extract molten glass for moulding. The Tank has a load of 600 kW connected across R and S phases. The Forehearth has a load of 720kW spread across the three phases. The function of the balancer is to deal with the unbalance due to the Tank load.

6.3.2 Layout and Components

The balancing system is divided into two separate but identical units, each capable of balancing 60% of the normal running load. This was done in order to allow planned maintenance to be carried out.

Each unit consists of five capacitor / inductor sections and one pilot-motor. Both capacitors and inductors are rated for 25 kVAr, 400 volt (capacitor maximum 480 volt). The motors used were ABB type N2BA 132 315 SMB, rated 132 kW at 400 Volt with 95.3% efficiency, and at 0.80 power factor.

For these motors, manufacturers test data indicated that

- $Z_1 = 0.66 + j1.83$
- $Z_2 = 0.031 + j0.15$
- Rated current is 254 amps at 0.85 power factor

6.3.3 Design Calculations

Running the balancer programme software produced optimum values of

A = 0.225 V and B = 0.155 V (See appendix B)

Maximum capacitor voltage with T phase removed was calculated to be 474 volts (neglecting motor saturation effects).

The maximum pilot-motor current was calculated at 273 amps.

Because the motor is designed for continuous running at 1% negative phase sequence voltage, it is capable of carrying I_S/I_N times 1% over-current, on one phase, on a continuous basis. This amounts to 7.5% over-current for this motor, and hence the rating of 254 amps can be increased to 273 amps provided the other phase currents are reduced by the appropriate amount.

6.3.4 Auto-transformer

The auto-transformer kVA rating was calculated as follows

- A section -- 49.6 amps, 11.2 kVA
- Centre section -- 56.7 amps, 43.9 kVA
- B section -- 272.7 amps, 42.3 kVA

For ease of manufacture and assembly the auto-transformers were constructed in two sections, one to provide the A voltage, the other the B voltage. In additions buck/boost transformers and variacs were added to each, in order to allow final adjustment. Figure 6.3 shows the connection diagram for this arrangement.

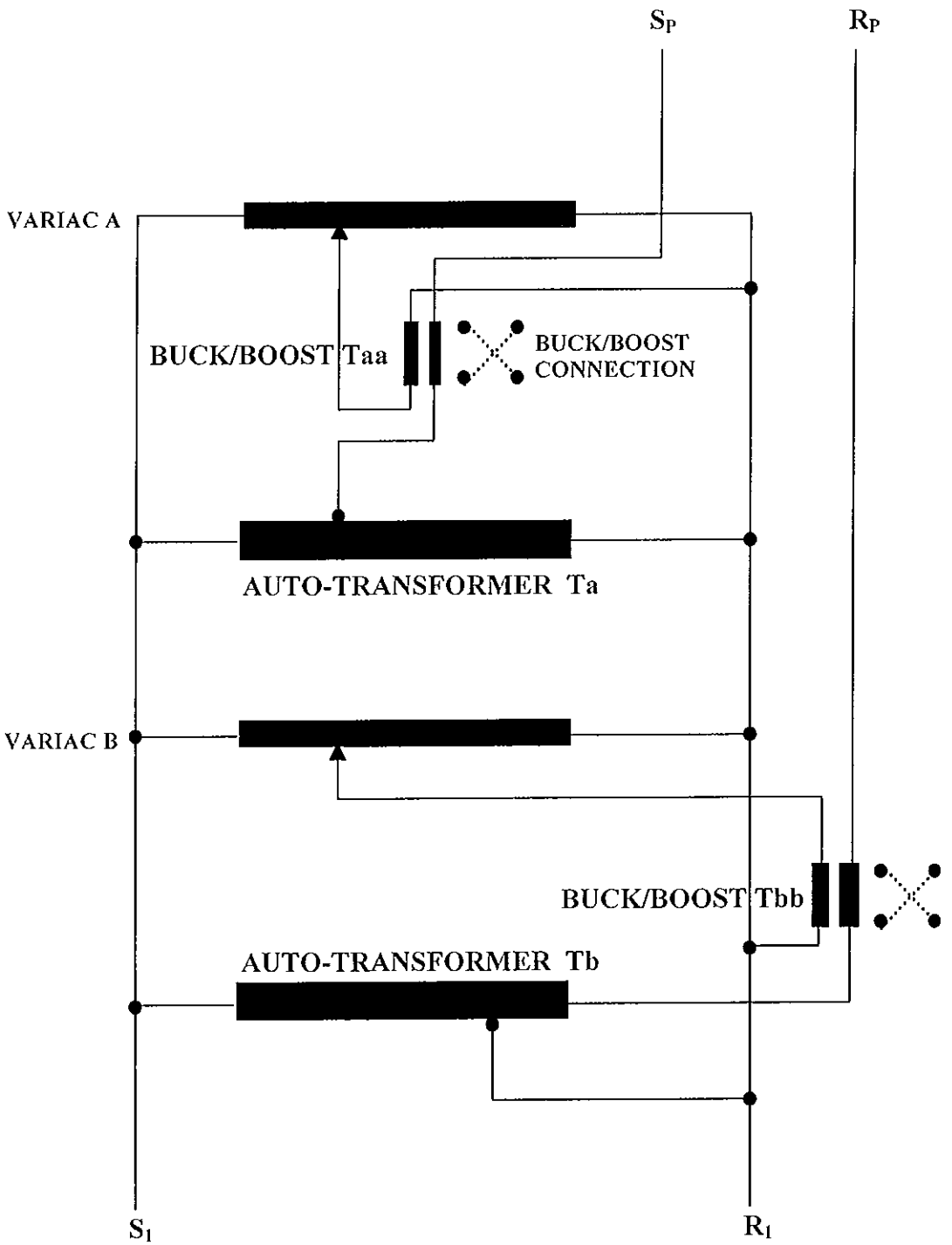


Figure 6.3 Auto-transformer arrangement

6.3.5 Motor Starting

Because of the large voltage drops caused, utility requirements and electrical standards govern the method of starting of electrical motors. Generally motors larger than 10 kW require the fitting of some method of soft starting, such as star-delta or electronic interface.

The pilot-motors used in the production balancer are of such a size (132 kW) that some form of soft start was considered essential in order to minimise voltage drop, particularly when starting from standby generator supply. Run up time is not important for this application and hence it was decided that the most economical method of staring was to use a suitably sized three-phase choke.

The choke is connected in series with the unloaded motor until it reaches full speed. A contactor then bypasses the choke. This method works well with unloaded motors, where starting time is not important. The starting current can be limited to the desired level, without generating the high harmonic currents associated with an electronic soft-start unit. This method is relatively inexpensive and easy to install.

6.3.6 Final Layout

Figure 6.4 shows in block form the balancer component layout.

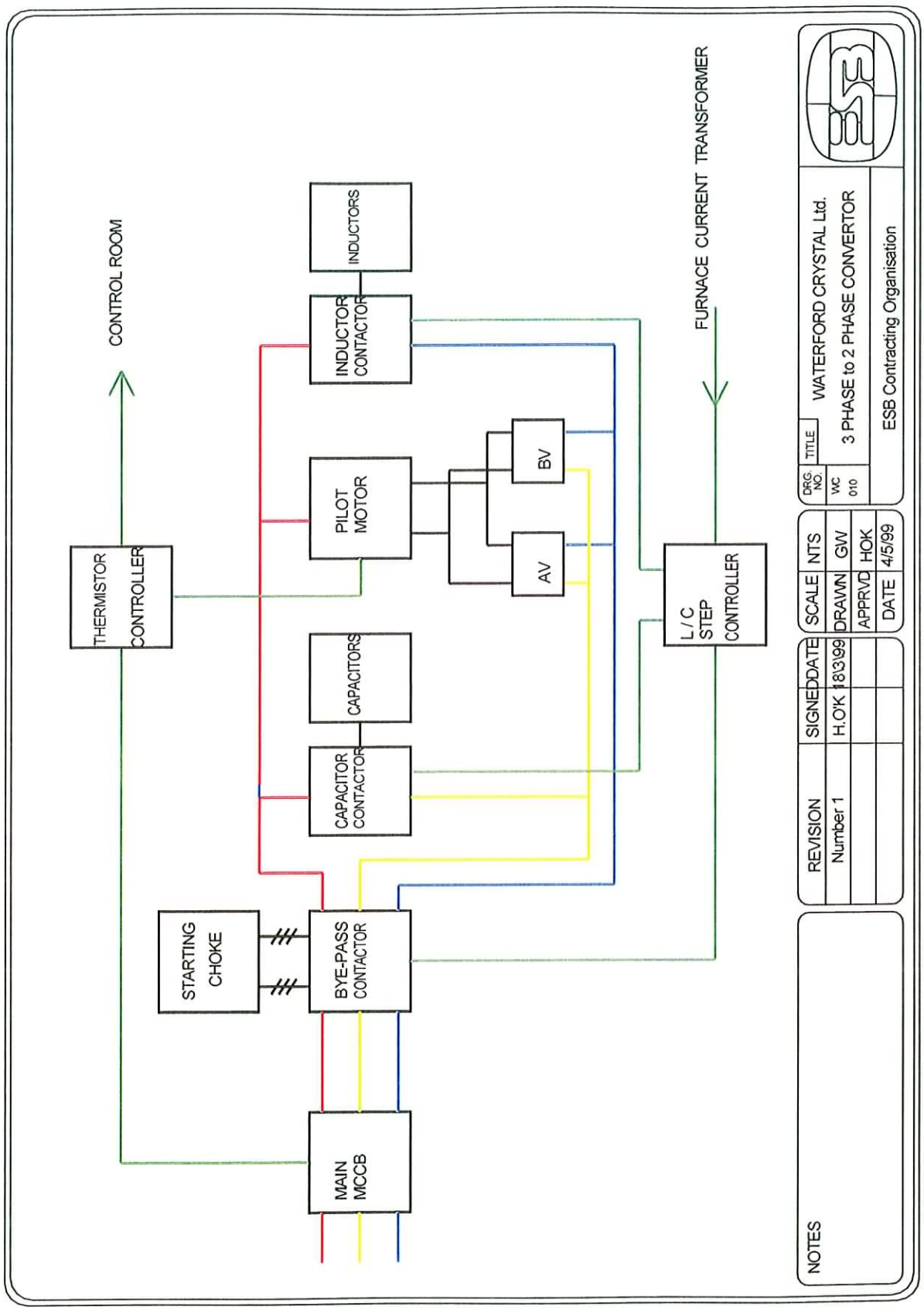


Figure 6.4 Balancer Block Diagram

Appendix E shows in photographic detail the construction of the production unit.

The two motors were arranged to rotate in opposite directions on a common mounting frame. This was done to reduce noise and vibration, by cancellation. The photographs show the motor assembly, and also the main balancer panels and auto-transformers. In addition there are photographs of the main switchboard showing the circuit breakers for the load, balancer and main supply taken in January 2001. The balancing of the phase currents can be seen from the respective ammeter readings.

6.3.7 Evaluation of motor balancer

6.3.7.1 Performance on Mains Supply

The results of the production balancer testing are shown in appendix F. The furnace load at the time of measurement was 560 kW, as indicated by the control room instrumentation.

The load, plus balancer currents, as measured by a Dranetz PPI were:

I_R = 1160 amps
I_S = 1143 amps
I_T = 1155 amps

The power factor of the three-phase currents was 0.71.

The voltages measured at the load side of the supply transformer were

R-S = 406 volts
S-T = 407 volts
T-R = 403 volts

From calculation this result gives a value for negative phase sequence voltage of 0.59%. This is within the required 2% required under Quality of Supply Standard EN50160 [2], and within the 1% required under IEC [1] for motors run long-term at full load.

6.3.7.2 Performance on Standby Generator Supply

When the load was changed over to the standby generator, the currents differed only slightly, as shown in appendix G; however there was some increase in percentage voltage negative phase sequence, as was expected with the higher source impedance.

The voltages measures at the generator terminals were

R-S = 401 volts
S-T = 405 volts
T-R = 398 volts

From calculation this gives a value of negative phase sequence voltage equal to 1.01%

Balance was well controlled with the capacitor/inductor steps following change in load. The negative phase sequence voltage was well within the 2% values required under EN50160 [2] standard, and was within the 1.5% required under IEC [1] standards for motors run short term at full load.

6.4 Conclusions

6.4.1 Performance

In terms of overall performance the balancer has improved the reliability of the furnace system. Voltage unbalance is controlled. Mains supply outages do not pose the voltage unbalance problems experienced in the past. Supply from standby generation does not lead to severe voltage unbalance and production can continue as normal.

6.4.2 Reliability

The balancer has proved to be very reliable. This unit was commissioned in the Autumn of 1999, and has been operation continuously since then. Maintenance is carried out annually. Measurement of the currents and voltages confirm the continued accuracy of operation. No adjustment has proved necessary over this period. Thermographic studies of all components have shown no overheating within the balancer. Testing of the pilot-motors indicates no significant deterioration or wear. The balancer step controller was on all occasions found to be operating reliably.

6.4.3 Customers Perspective

From the client's point of view, the balancer has allowed increased flexibility in the connection and relocation of production equipment. Load can be connected to the furnace supply for optimum production performance. Production managers no longer have to concern themselves with the question of the overall electrical phase balance of the furnace.

6.4.4 Practicality of design

During the design of the prototype and production models, pilot motor balancers were constructed and tested using six motors (two prototype 7.5 kW and four production 132 kW motors).

It was found that the measured locked rotor and no load impedances varied from that provided by the motor manufacturers. Although these variations were not large their effect on the required A and B ratio's of the auto-transformers was significant.

The result was that each motor had to be measured separately and the auto-transformers had to be independently adjusted for that motor. This was a very time consuming activity and it was generally necessary to carry this adjustment out several times before a final satisfactory result was obtained with a particular motor. This requirement would be a costly and inconvenient overhead for the continuous production of this type of balancer.

It was therefore decided to revisit the capacitor/inductor method, as this seemed from initial assessment, to be more suitable for standardised design and construction.

CHAPTER 7

CAPACIOR / INDUCTOR METHOD, A FRESH APPROACH

7.1 50 Hertz Resonance Problem

The main problem with past attempts to use Capacitor / Inductor method related to the danger of 50 Hz resonance in the event of the centre phase (T phase in this case) becoming disconnected. This leads to the occurrence of a short circuit between R and S phases as shown in Figure 7.1.

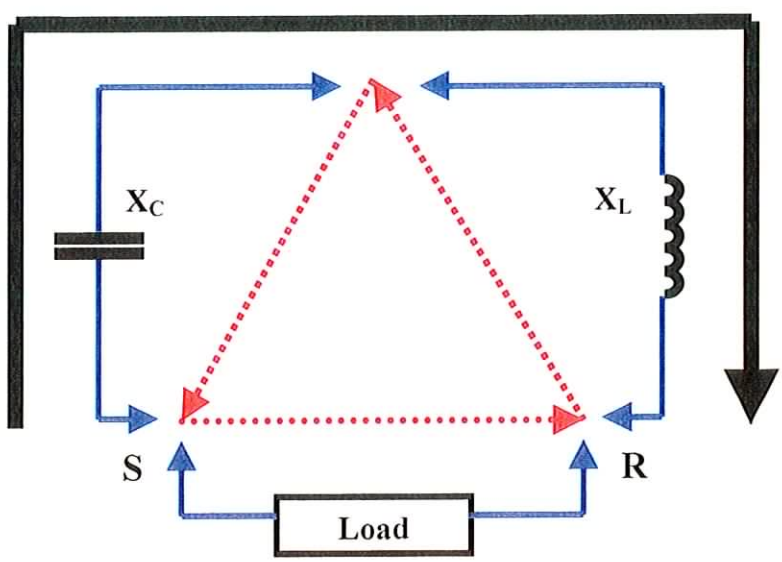


Figure 7.1 50 Hertz resonant circuit

The capacitor voltage is given by

$$Vc = \frac{VRS \times XC}{(XL + XC)}$$

In theory the capacitor voltage reaches infinity as $X_L + X_C$ approaches zero. In practice, if iron cored reactors are used, saturation will take place and limit the voltage rise. In order to determine typical voltage rise levels an experiment was conducted with standard industrial components and the currents measured and analysed.

7.2 Measurement of Over-Current and Voltage-Rise

A laboratory experiment was set up to measure over-current and over-voltage in the event of centre phase loss with a capacitor/inductor balancer. The following is an outline of the experiment.

7.2.1 Purpose of experiment

The purpose of the experiment was to determine the current flow and associated voltage rise when a capacitor and iron cored inductor are series connected and tuned to 50 Hz and are connected across a 400 volt supply.

7.2.2 Equipment used

I. One iron cored inductor as manufactured by Hans Von Mangoldt, Aachen, Germany having a value of 68 milli-Henry, and a voltage rating of 440 volts, giving a rating of 10 kVAr, and a continuous current rating of 25 amps.

II. Four three-phase 15 kVAr capacitors rated at 400 volts, and internally connected in delta, as manufactured by Nokian Capacitors Limited of Finland. Two of the three-terminal connections were commoned to convert the capacitor into a single-phase unit of 10 kVAr. As the voltage stress was likely to cause more serious damage to the capacitor than the reactor, the former were arranged in a series parallel combination in order to give the same kVAr rating at double the voltage withstand level (800 V, see Figure 7.2).

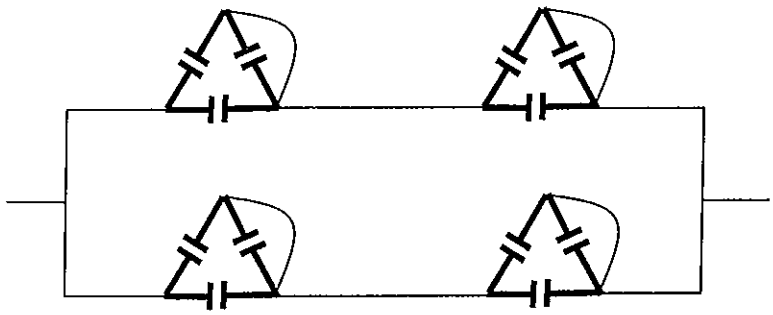


Figure 7.2 Test capacitor connections

III. One switchboard supply point, rated at 800 amps continuous and controlled by a Moulded Case Circuit Breaker (MCCB).

IV. Dranetz PP1 power analyser fitted with motor inrush software and memory card [16].

V. IBM PC with Dranview Power Analysis software [16].

7.2.3 Measurement Procedure

The test circuit was as shown in Figure 7.3. The circuit was located behind a screen, in order to provide personal protection in the case of violent capacitor failure. The control point was screened from the circuit location.

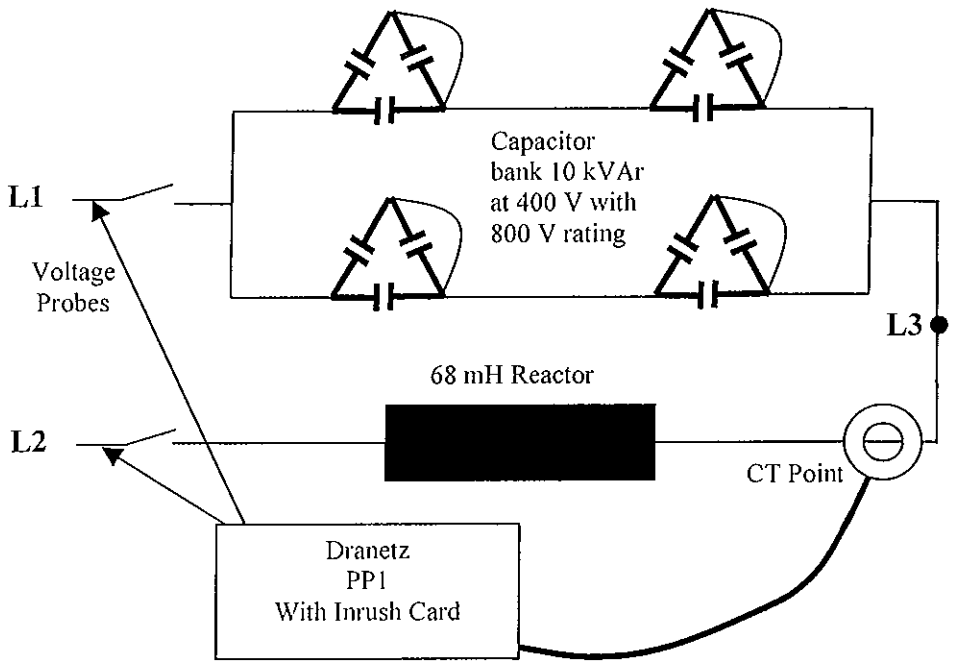


Figure 7.3 Test circuit

An initial test was undertaken to determine the current after switching. From this the likely voltage at point L3 was calculated so as to ensure the voltage-test instrument would not be over-stressed. A current of 136 amps was recorded. With a capacitor power of 10 kVAr at 400 volts giving an impedance of 16 ohms, this was roughly estimated to give rise to a voltage of 2176 volts. As this was in excess of the instrument specification of 1000 volts, it was decided to measure the current and calculate the corresponding voltage.

The following results were obtained during the test. Figures 7.4 show the complete current envelope and Figure 7.5 the steady state portion of the curve.

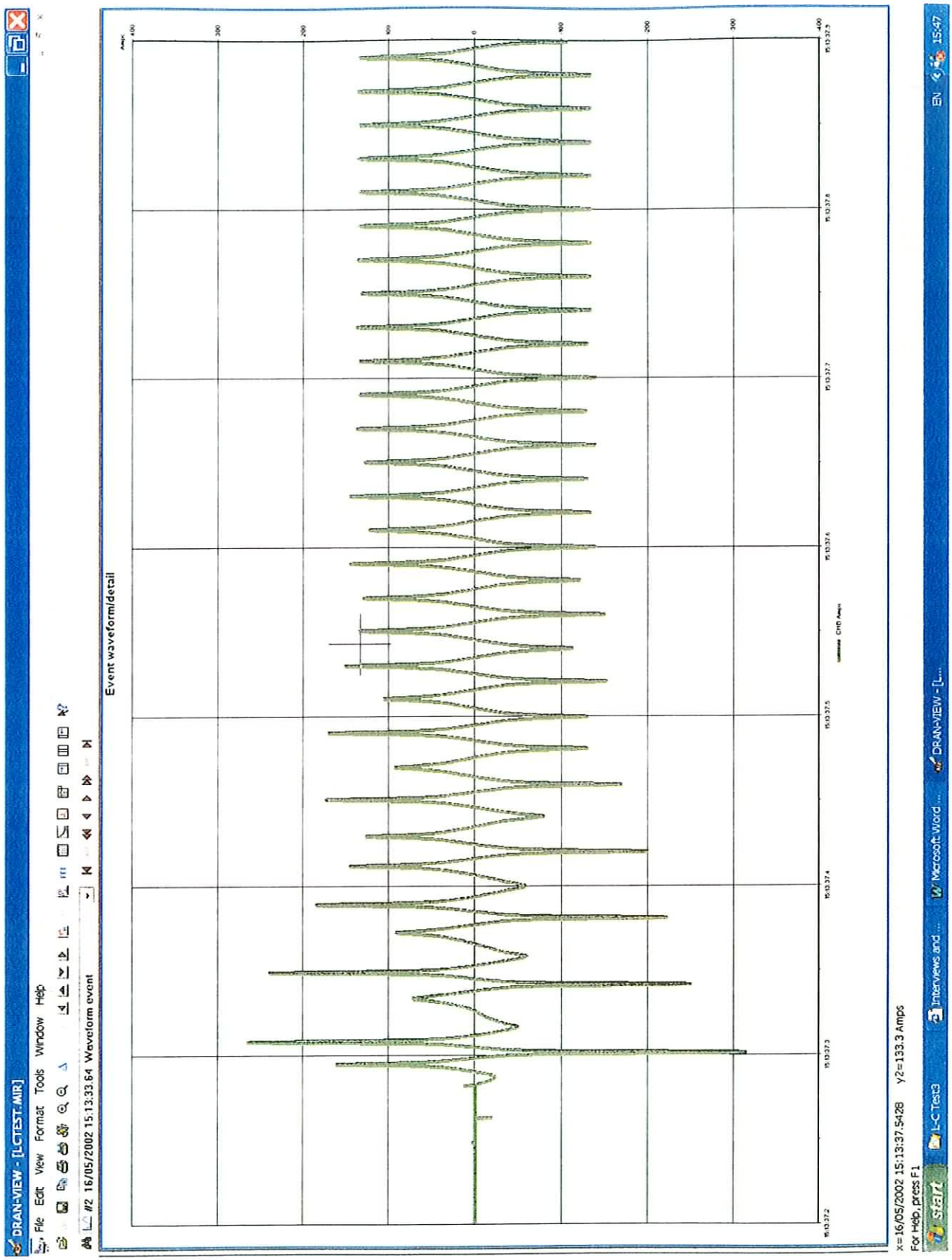


Figure 7.4 Current taken during test including inrush and steady state.

Figure 7.5 Steady state current after inrush has stopped

Table 7.1 shows the harmonic breakdown of the steady state current. Capacitor impedances are added to this Table and from this the corresponding harmonic voltages are calculated. These voltages are added arithmetically (assuming worst case conditions), to arrive at the total peak voltage.

Calculated Capacitor Voltage from Capacitor Impedance

Note: Assumes peak co-incidence.

Harmonic Number	Capacitor Impedance	CHA Amps	Calculated Voltage	Harmonic Number	Capacitor Impedance	CHA Amps	Calculated Voltage
FND	16.000	55.947	895.152	28	0.571	0.048	0.027
2	8.000	0.004	0.032	29	0.552	0.022	0.012
3	5.333	19.287	102.864	30	0.533	0.078	0.042
4	4.000	0.069	0.276	31	0.516	0.048	0.025
5	3.200	10.455	33.456	32	0.500	0.013	0.007
6	2.667	0.022	0.059	33	0.485	0.078	0.038
7	2.286	5.564	12.718	34	0.471	0.056	0.026
8	2.000	0.056	0.112	35	0.457	0.069	0.032
9	1.778	2.543	4.521	36	0.444	0.004	0.002
10	1.600	0.069	0.110	37	0.432	0.043	0.019
11	1.455	1.458	2.121	38	0.421	0.022	0.009
12	1.333	0.061	0.081	39	0.410	0.026	0.011
13	1.231	0.625	0.769	40	0.400	0.017	0.007
14	1.143	0.065	0.074	41	0.390	0.004	0.002
15	1.067	0.234	0.250	42	0.381	0.078	0.030
16	1.000	0.061	0.061	43	0.372	0.009	0.003
17	0.941	0.174	0.164	44	0.364	0.135	0.049
18	0.889	0.039	0.035	45	0.356	0.009	0.003
19	0.842	0.195	0.164	46	0.348	0.004	0.001
20	0.800	0.052	0.042	47	0.340	0.03	0.010
21	0.762	0.234	0.178	48	0.333	0.135	0.045
22	0.727	0.039	0.028	49	0.327	0.03	0.010
23	0.696	0.1	0.070	50	0.320	0.178	0.057
24	0.667	0.017	0.011				
25	0.640	0.056	0.036		**Voltage Peak**		**1053.457**
26	0.615	0.069	0.042				
27	0.593	0.052	0.031				

Table 7.1 Harmonic Breakdown of Capacitor Current taken from Dranetz Software.

Result:

I. Peak voltage rating of capacitor exceeded by a factor of 1.86 (capacitor rated at 400 V RMS, 565 V Peak)

II. Measured steady-state current of 55.95 amps + Total Harmonic Distortion of 22.87 amps, giving a total seady-state current = 60.44 amps.

III. Current rating of capacitor exceeded by a factor of 2.41 (capacitor rated at 25 Amps)

The laboratory tests show that, using this type of reactor, the capacitor peak voltage rating would be exceeded by a factor of 1.86, while the steady state current rating would be exceeded by a factor of 2.41.

7.2.4 Conclusions

It was concluded that the removal of the central phase would result in a high possibility of the capacitor being over-stressed, with the consequent possibility of violent failure. It was therefore deemed necessary to take account of this fact in the design of any balancer built using Capacitor / inductor combinations.

7.3 Contactor Bounce & Phase Loss

A practical balancer will have several automatically controlled stages, switched by contactor in order to follow load variations. Central phase loss can arises for a number of practical reasons. These include:

I. Contactor bounce or contact closure/opening timing variation within isolators or switchfuses. *This problem does not normally affect load. However the 50Hz resonance tests shows that a high inrush takes place when the centre phase becomes disconnected momentarily. The magnitude of the voltages impressed upon the capacitor would be likely to cause failure.*

II. Fuse failure within the balancer banks

III. Supply phase failure

7.4 Phase Loss Solution and Safety Issues

It was decided that a capacitor/inductor balancer could be built if sufficient safeguards were taken against the possibility of centre phase disconnection and consequently the possibility of violent capacitor failure. A number of safeguards were identified for this project. These included:

I. Contactor wiring arrangement to prevent centre phase disconnection by contact bounce or delayed closure / early opening of this phase connection. This is achieved by bypassing the contacts carrying the centre phase, so that in normal operation this phase is left permanently connected.

II. The installation of the capacitors within a locked and controlled caged compound, with suitable electrical door interlocking, warning instructions and access limited to trained maintenance personnel.

III. The use of a maintenance operating procedure, which would ensure that balancer steps are switched off by contactor before the associated circuit breakers are opened.

IV. Insertion of an impedance between the centre and other phases in order to prevent excessive voltage rise in the case of loss of centre phase. This is achieved by the connection of a suitable unloaded motor, which must be connected before the balancer can be switched on.

V. The use of an under-voltage tripping device on the main supply circuit breaker in order to sense and operate on loss of phase.

VI. The use of an over-voltage tripping device on the main balancer panel circuit breaker.

7.5 Example of a Practical Solution

7.5.1 The Furnace Load

The furnace consists of three separate sets of phase to phase loads of different and varying value. These loads comprise pairs of electrodes located (a) in the main melting chamber and (b) in production channels attached to this melting chamber. The schedule of loads as shown in appendix H was then re-distributed. The purpose was to achieve the best balance possible of the existing supply; so as to reduce the size of the balancer required.

7.5.2 Solution Design

The solution involves two separate balancers combined in one housing. Each balancer operates on a separate phase pair. The largest balancer was connected to the phase pair with the highest load, the other to the second highest loaded pair, with no balancing being required for the third pair.

The calculation of optimum load re-distribution and balancing was carried out using a Microsoft Excel spreadsheet as set out in Figure 7.1. The three tables on the left show how 1080 amps of load connected between L1 and L2 is first balanced to give 623 amps per phase. 325 amps of load connected between L2 and L3 is then balanced to give 187 Amps per phase.

The boxes and arrows pointing two these two stages show the capacitor / inductor steps required in order to arrive at the balance shown.

Step controllers controls the balancer and the boxes on the right refer to the current control settings for each step. These currents are measured using two 2500/5 amp current transformers, located at a suitable measuring location, on the furnace supply circuitry. The 5 amp secondaries of the current transformers are connected to proprietary digital current sensing controllers as manufactured by Zurc of Barcelona, Spain..

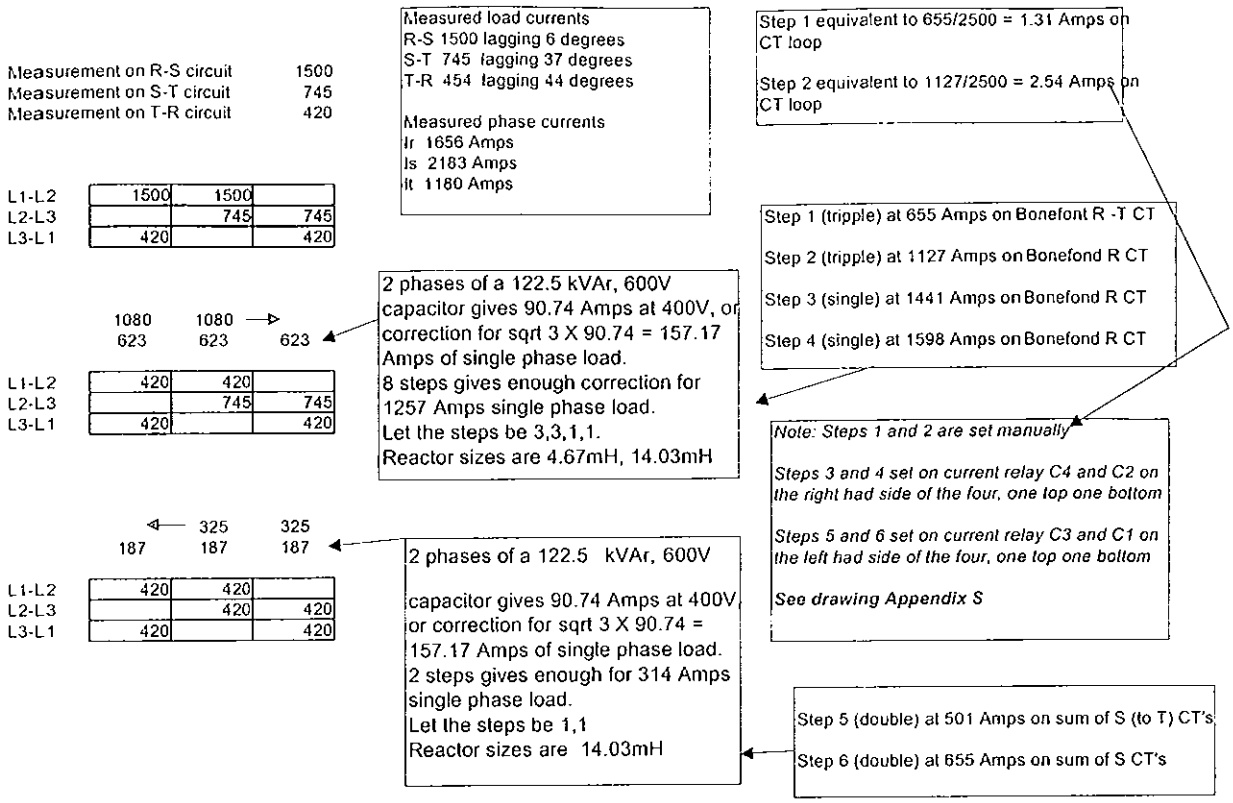


Table 7.1 Load balancing procedure

The balancer steps were constructed in two sizes
A. Sized to balance 471 amps of two-phase load
B. Sized to balance 157 amps of two-phase load

The larger sizes are designed for use during furnace start-up and the smaller steps were designed to follow the normal operating range of the load. The steps were dimensioned so as to give a maximum negative phase sequence voltage of less than 1%, this being the level above which motors must be de-rated according to IEC 60034-1 [1].

The effect of each step depends upon value of the source impedance and the calculation was carried out both for utility and standby generator supply. Table 7.2 shows the calculated values of increased percentage negative phase sequence of voltage, arising from the connection of balancer steps A or B, with either the utility or generation supply connected. The calculation process is shown in Figure 7.3.

Source	Step size A % NPS V	Step size B % NPS V
Utility (0.00139 +j0.00733 Ω, (as given)	0.51	0.17
Generator (0 + j0.065 Ω, (as given)	1.12	0.37

Table 7.2 Resulting increase in %NPS Voltage

It can be seen that with the worst case scenario, a large step on standby generator supply, a maximum of 1.12% voltage negative phase sequence is caused.

Effect of two phase load on voltage unbalance	
enter data in orange, answer in blue	
2 Phase Load kVA	108.878
Power factor	0
Voltage	400
Amps	272.195
I_R	272.195
I_2	136.0975+78.5759282610351i
I_{R2}	136.0975+78.5759282610351i
I_{S2}	-136.0975+78.5759282610351i
I_{T2}	4.2632564145606E-014+157.15185652207i
I_1	136.0975-78.5759282610351i
I_{R1}	136.0975-78.5759282610351i
I_{S1}	-136.0975-78.5759282610351i
I_{T1}	4.2632564145606E-014+157.15185652207i
Calculated Short Circuit Power (MVA) at Trafo LV terminals	9.69
R/X ratio	0
Z	0.016511868
X	0.016511868
R	0
Z complex	1.65118679050568E-002i
Delta V1	1.29743534796343+2.24722394220847i
Delta V2	-1.29743534796343+2.24722394220847i
Delta VR	4.49444788441694i
Delta VS	-4.49444788441694i
Delta VT	-2.66453525910038E-015i
Balanced Voltage Vrs	400
Balanced Voltage Vst	-200-346.410161513776i
Balanced Voltage Vtr	-200+346.410161513776i
Unbalanced Voltage Vrs	400+8.98889576883388i
Unbalanced Voltage Vst	-200-350.904609398193i
Unbalanced Voltage Vtr	-200+341.915713629359i
Positive Phase Seq V	201.297435347964-113.2228298957 17i
Absolute V_1	230.9546854
Negative Phase Seq V	-1.2974353479635-2.24722394220859i
Absolute V_2	2.594870696
% NPS Voltage	1.12%

Table 7.3 – Load unbalance calculation results for a three capacitor step combination (example of 3 by 90.94 amps giving 272.195 amps)

7.5.3 Capacitor Over-Voltage Calculation

It was decided to introduce impedance between the centre phase (T phase) and the other two phases in order to limit the capacitor voltage in the case of T phase becoming disconnected. This was achieved by connecting idling asynchronous motors in such a way that the balancer would not function unless these were running.

Two motors were installed for this purpose. Only one is required, the other acts as a standby.

The motors used were ABB catalogue number N2BA 132 315 SMB, rated 132 kW at 400 volt with 95.3% efficiency, and at 0.80 power factor. For these motors, manufacturers test data indicated that

- $Z_1 = 0.66 + j1.83$ ohms
- $Z_2 = 0.031 + j0.15$ ohms

Rated current is 254 amps at 0.85 power factor

Z1 and Z2 are the positive and negative phase sequence impedances of the motor running under no-load.

In the worst case situation a capacitor voltage of 887 volts can be reached as shown using the balancer programme appendix A. This is within the short term withstand capability of the capacitor, and will also cause the main balancer circuit-breaker on over-voltage, after a short period. The programme output for this calculation is shown in appendix K.

7.5.4 Balancer Construction & Installation

The balancer is wired as shown in appendix I. The balance control panel was constructed to IEC and ETCI standards for safety and reliability.

The balancer consists of two sections:

a) A switchboard containing all circuit-breakers, isolators, switch-fuses, contactors and controls.

b) A locked and controlled caged compound, located behind the main panel and containing all capacitors and inductors (see photographs, appendix J)

Within the switchboard are contained the current sensing relays which are set to the calculated switching levels as set out in Table 7.1.

7.5.5 Commissioning & Testing

The commissioning test consisted of three stages:

I. Voltage and current injection testing

II. Test of balancer under no furnace load conditions

III. Test of combined balancer/furnace load

The test details are as follows;

I. A voltage injection test was carried out on all balancer wiring using a Megger instrument. The controlling relays were tested using current injection to ensure that they were operating correctly.

II. Testing was carried out with no furnace load connected. The balancer was forced to its maximum setting on the larger of the two balanced circuit (290.37 kVAr at 400 volts)). Measurements were then taken of system voltage and phase and these values used to calculate the negative phase sequence voltage component. The measured value was then compared with that calculated by the balancer programme. The results of this test are shown in appendix L and indicate that Vnps = 2.94%. The calculated value as shown in appendix M is Vnps = 2.99%. (Minor variations in source impedance are normal on utility systems due to changing supply network arrangements. This and the impedance of connected load will lead so some variation in results.)

III. Tests were conducted using the combined load, furnace and balancer. These results shown in appendix O indicate that the negative phase sequence current had reduced from 40.49% (appendix N) to 16.18%.

7.6 Conclusions

7.6.1 Performance

The Capacitor / Inductor balancer has been installed since early 2001, and has been operating successfully. In terms of overall performance this balancer is performing as well as it's rotary equivalent. Mains outages have not posed any problems and the system operated well under generator supply. The balancer has enabled production to continue without supply quality problems while being supplied by the standby source.

7.6.2 Reliability

The balancers have proved to be very reliable. The balancer was commissioned in May 2001, and has been operation continuously since then. Maintenance is carried out annually. Measurement of the currents and voltages confirm the continued accuracy of operation. No adjustments have proved necessary over this period. Thermographic studies of all components have shown no overheating within the balancer. The balancer step controller was on all occasions found to be operating reliably.

7.6.3 Customers Perspective

From the client's point of view, the balancer has allowed increased flexibility in the connection and relocation of production equipment. Loads can be connected to the furnace supply for optimum production performance. During furnace rebuild balancer steps may easily be transferred to different phase pairs to suit a revised production process. Because of the flexibility of the Capacitor/Inductor balancer, Production Managers no longer have to concern themselves with the question of the overall electrical phase balance of the furnace.

7.6.4 Practicality of design

The Capacitor/Inductor method proved very flexible in design and operation, consistent in performance and requires little maintenance. Once sufficient care is taken to prevent a 50 Hertz series resonance, this method seems most suitable for the balancing of any large load.

CHAPTER 8
HARMONIC DISTORTION PROBLEMS

8.1 Thyristor Controlled Elements

The use of an electronic interface between supply and load is a common feature of most modern electrical load and electrical glass furnaces are no exception. The purpose of this electronic interface is to improve the efficiency and control of the system in question.

For electrical glass furnaces temperature is critical in order to achieve the correct level of viscosity. The viscosity of the molten glass is important in determining malleability during the blowing process and the quality of the final blown product.

Within most glass furnaces control is achieved either by the use of large motorised regulators, or by thyristor phase angle control of the currents passed through the elements. In this instance both systems are in use, with the 'Tank' (or pre-heating area) controlled by regulator and the 'Forehearth' (working area) controlled by of use of thyristors, for more accurate adjustment. As the latter consumes about 60% of the power, harmonic distortion caused by the thyristor switching process becomes a major issue. This needs to be addressed in order to prevent other essential equipment from being adversely effected.

8.2 Harmonic Measurements

Distortion measurements were carried out after the furnace was running and the voltage distortion levels were found to be above G5/4 planning levels [7]. As these levels are selected to minimise the possibility of problems for connected load; it was decided that the measured levels should be reduced by the application of suitably designed passive filters.

Harmonic distortions arising from thyristor load behave as current generated sources, within the normal range of voltage distortion levels experience on public utility networks, i.e. within the range 0% to 10%. Therefore in order to determine the type of

filtering required and to allow the dimensioning of components, it was first necessary to measure the harmonic currents being generated by the load during normal operation. This was carried out using a Dranetz PP1 Harmonic analyser [16], and the results are as shown in Figures 8.1 to 8.4. and in Table 8.1.

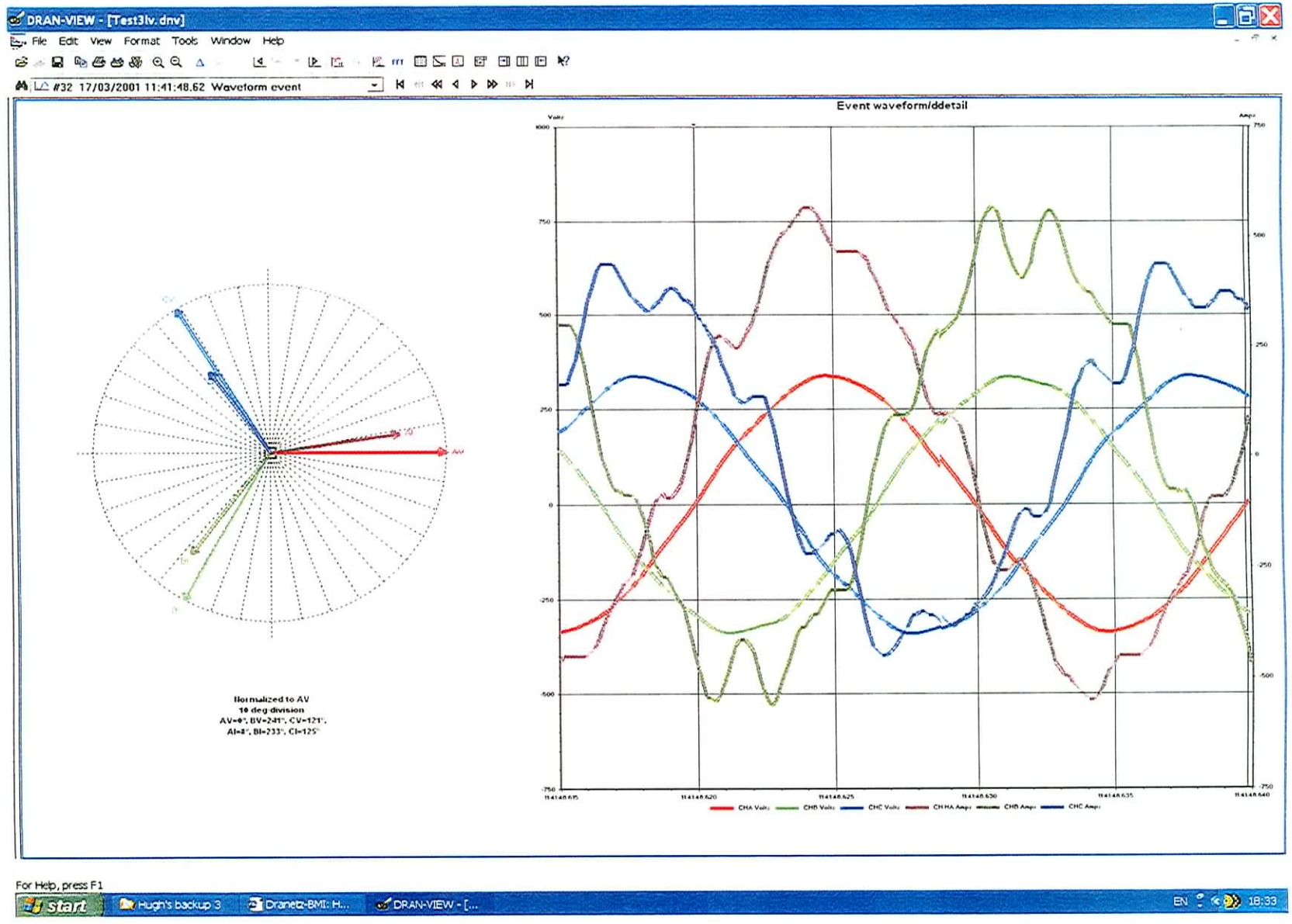


Figure 8.1 Harmonic Load Current – Balanced Furnace

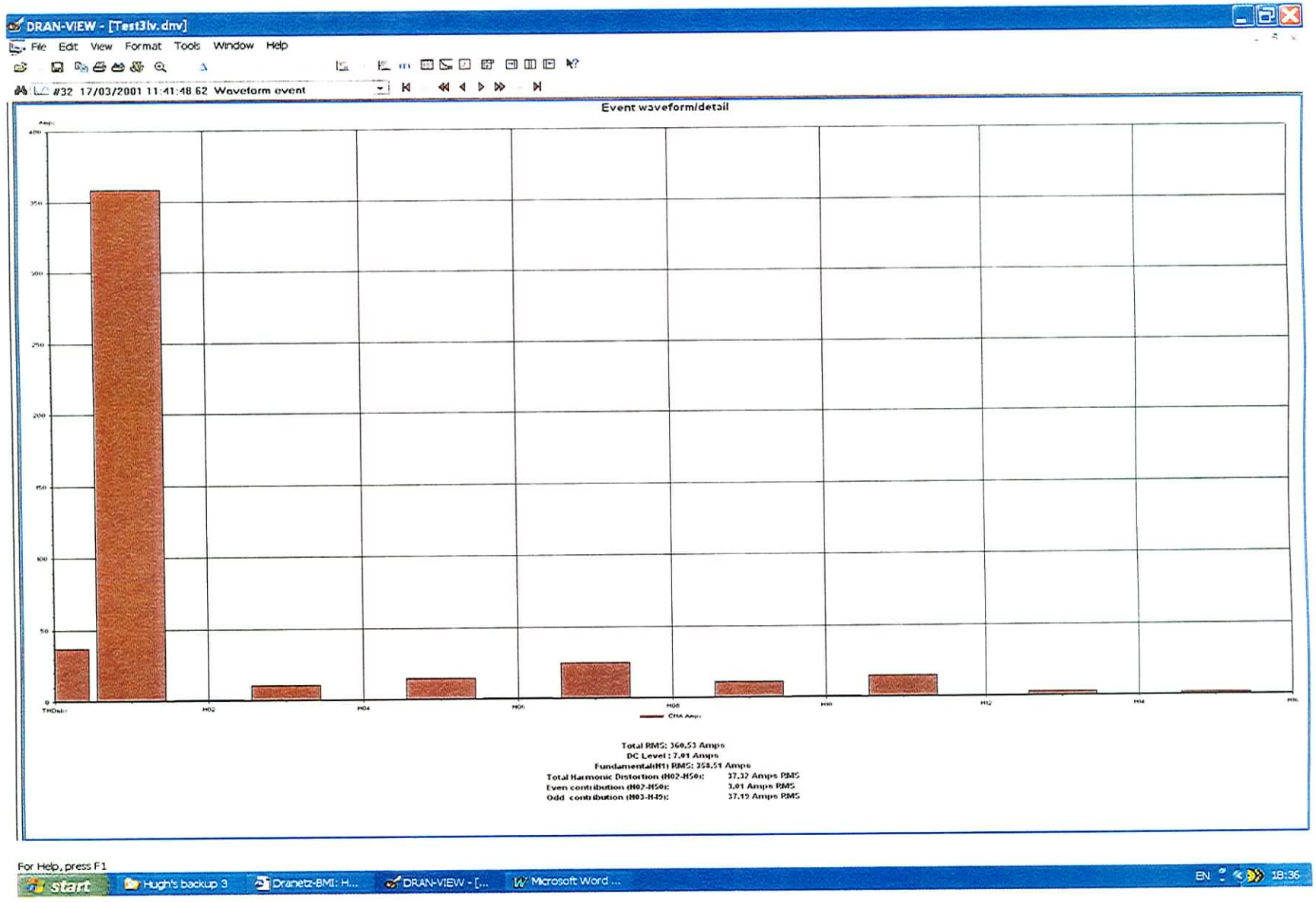


Figure 8.2 Spectrum of harmonic current R phase

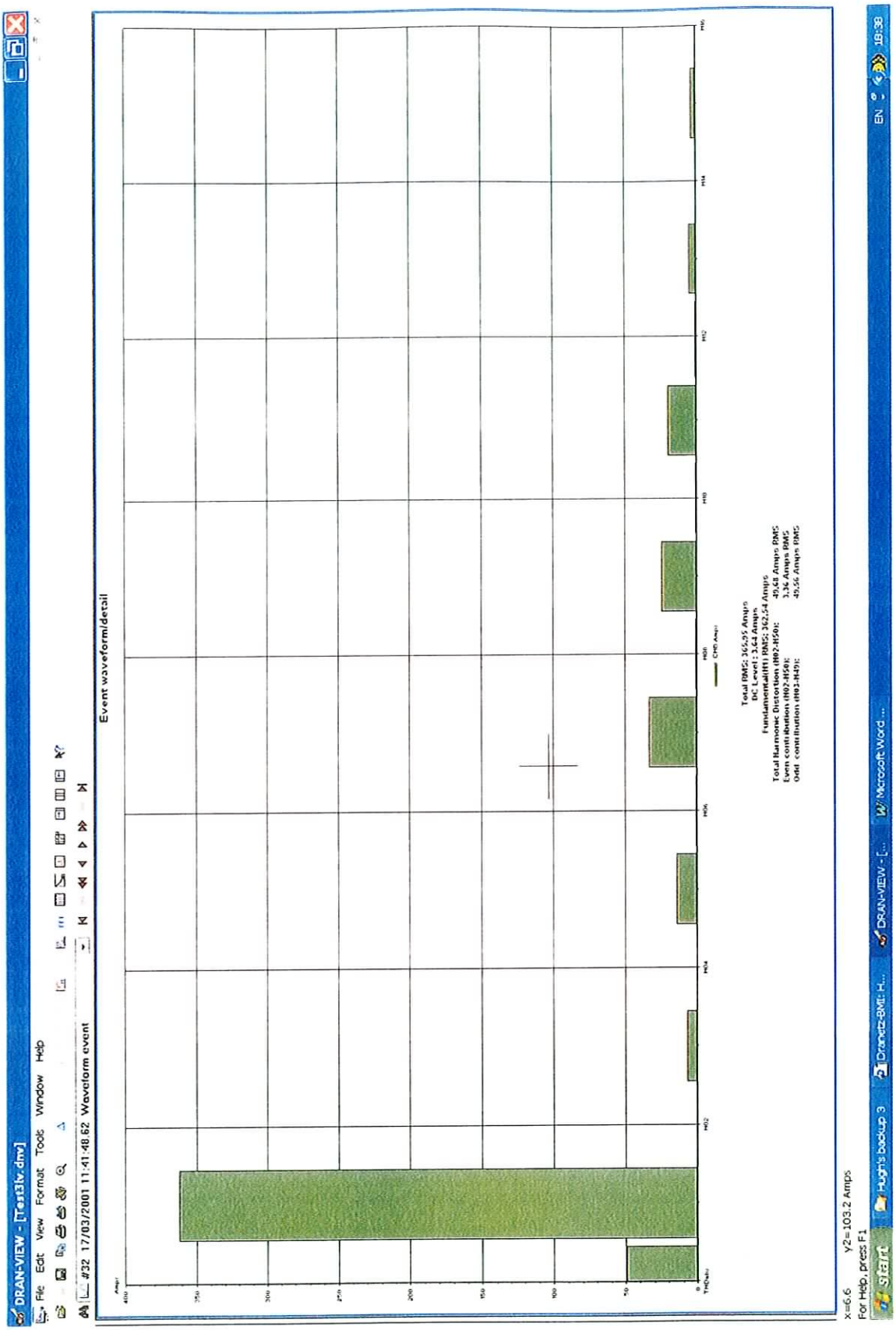


Figure 8.3 Spectrum of harmonic current S phase

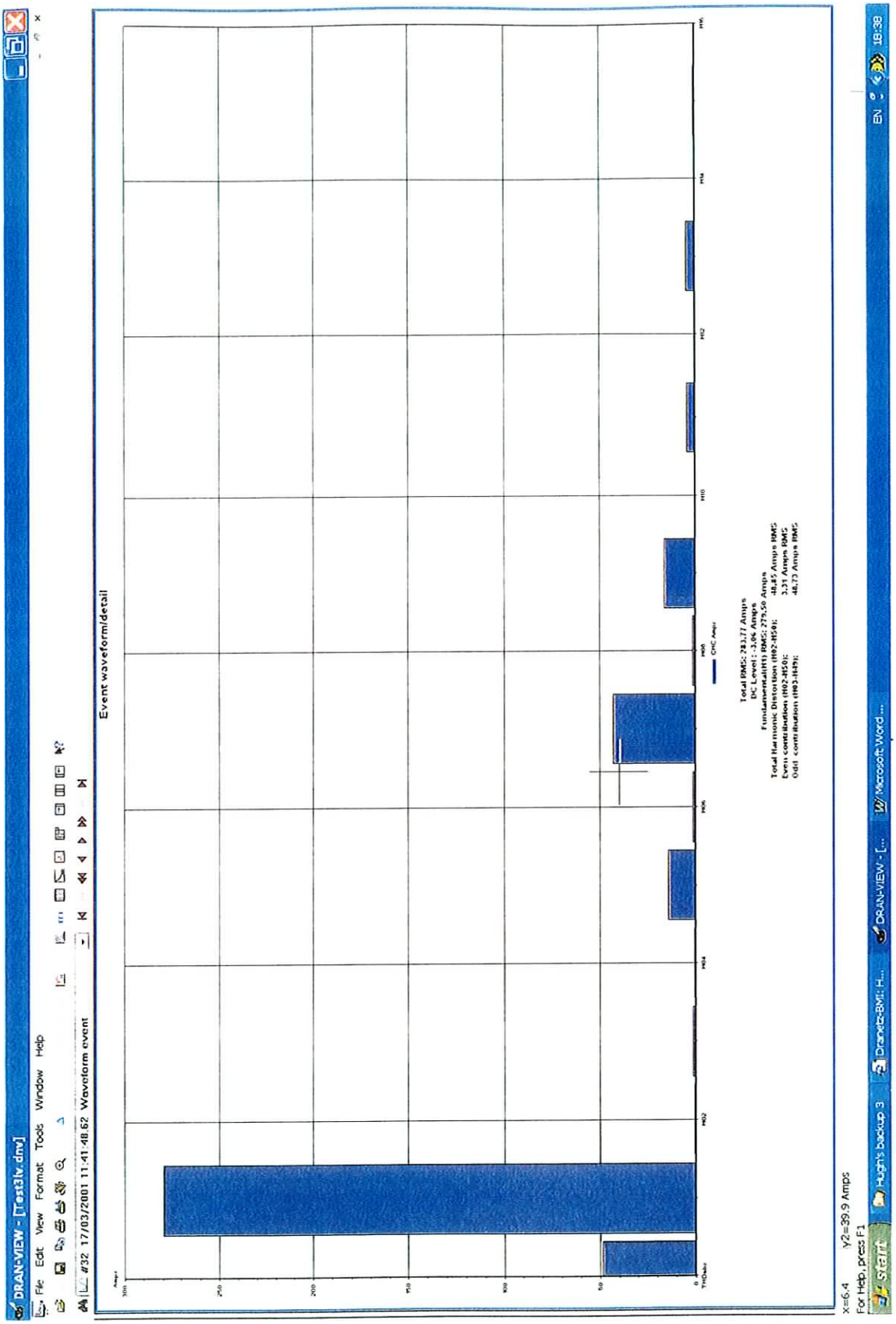


Figure 8.4 Spectrum of harmonic current T phase

	Channel R Volts	Channel S Volts	Channel T Volts	Channel R Amps	Channel S Amps	Channel T Amps
FND	235.1	236.49	235.71	1792.55	1812.7	1397.5
H02	0.07	0.05	0.04	6.05	3.55	3.3
H03	1.96	0.95	1.62	54.9	35.15	7.9
H04	0.01	0.04	0.11	2.2	2.85	4.2
H05	1.73	1.42	2.19	74.95	71.5	72.2
H06	0.14	0.16	0.28	5.85	5.7	7.5
H07	2.47	3.51	4.64	127.25	168.55	214.8
H08	0.03	0.1	0.17	2.65	4.8	8.2
H09	0.84	0.98	1.49	57.65	123.25	81.75
H10	0.06	0.05	0.06	5.75	5.35	2.1
H11	0.79	1.48	0.5	75.85	100.7	21.95
H12	0.02	0.01	0.04	3.45	4.8	1.6
H13	0.2	0.32	0.24	16.4	25.25	23.6
H14	0.03	0.05	0.03	1.95	2.7	0.5
H15	0.28	0.47	0.34	9.05	16.8	4
			R phase	S phase	T phase	
		Power Factor	0.990 Leading	0.992 Leading	0.998 Lagging	

Table 8.1 Table of Harmonic Voltages and Currents (furnace plus balancer)

8.3 Harmonic Measurement Results

The measurements indicate that large harmonic currents, dominated by the 5^{th}, 7th, 9^{th} and 11^{th}, circulate from the load back to the supply source. It would normally be expected that each harmonic current value would decrease in magnitude in proportion to the reciprocal of their number. However the presence of the balancing capacitors has the effect of causing harmonic resonance, which in this case amplifies the 7^{th}, 9^{th} and the 11^{th}.

8.4 Harmonic Filter Design

It was decided to design a passive filter bank to absorb the harmonic currents generated by the thyristor load. The filter was to consist of four branches, one designed to absorb the 3^{rd}, 5^{th}, 7^{th}, 9^{th} and 11^{th} harmonic currents.

Initial consideration was given to the design of an asymmetrical filter with three non equal branches. After consideration, this proposal was discarded in favour of a balanced filter for two reasons;

I. An asymmetrical filter would limit the flexibility of adding thyristor control across other phase pairs at a later stage.

II. Large single-phase capacitors would be required. These are non-standard and expensive.

8.4.1 Design Calculations

The process of designing a suitable filter involved considering the equivalent circuit, including supply source, harmonic generators, and filter branches. The objective was to calculate the current and voltages levels of all the components within this network so as to allow the proper component dimensioning, while absorbing the required harmonic current generated by the load. An equivalent circuit is shown in Figures 8.5.

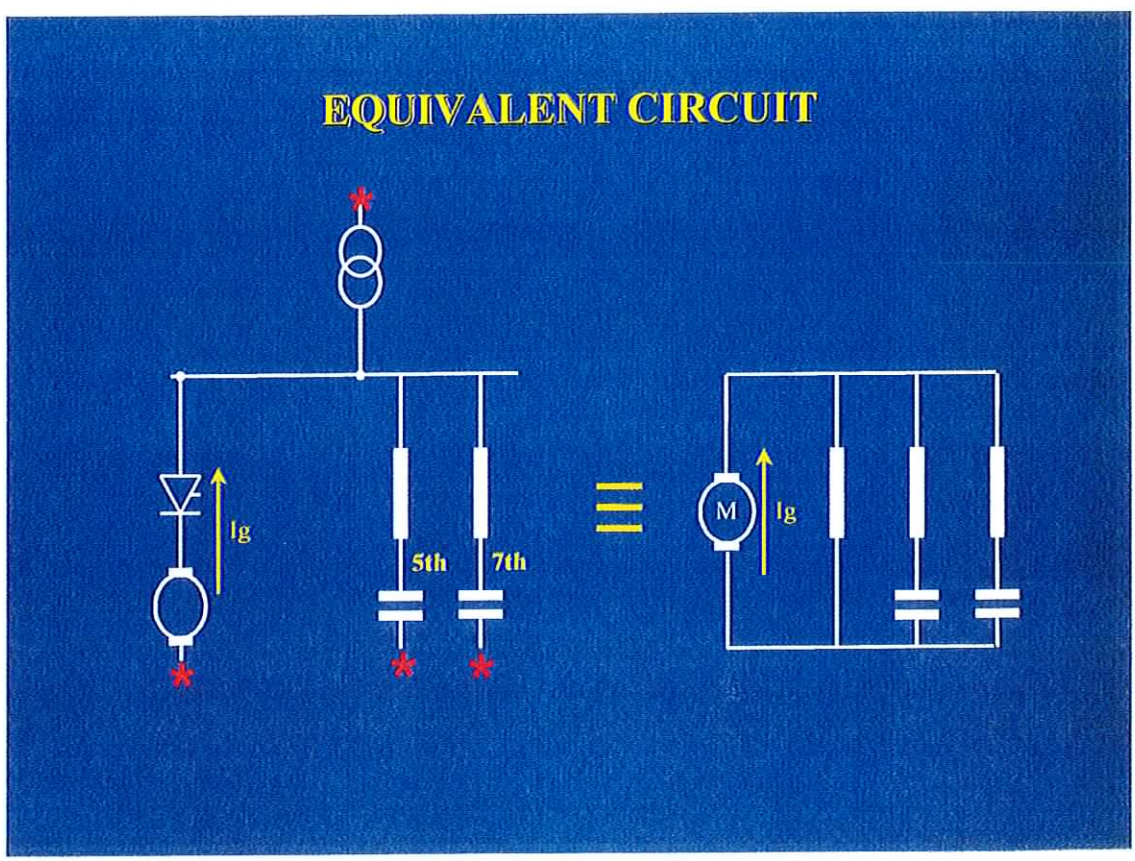


Figure 8.5 Typical equivalent circuit of a harmonic filter

The harmonic source may be treated as a current generator supplying three parallel impedances, the two filters and the supply source impedance.

The harmonic generator, the supply source and the harmonic filters may be treated as three-phase sources, connected to a common star equivalent point.

Each filter branch has an associated parallel and series resonance; as shown in Figure 8.6. The parallel resonance results in a high impedance to the flow of harmonic current whilst the series resonance results in a low impedance path.

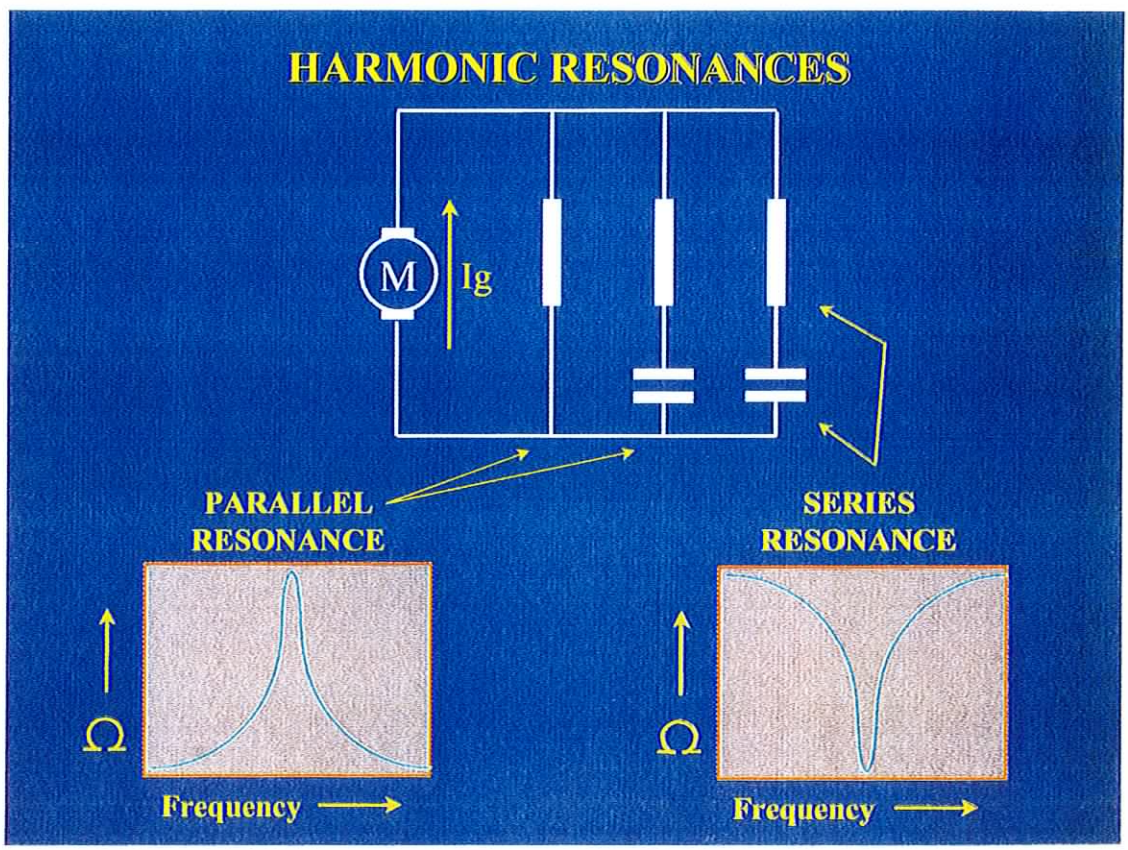


Figure 8.6 Parallel and series resonance points

By calculating the admittance of each branch it is possible to divide the generated current between the three branches. From this the current flow for each harmonic frequency for each branch may be calculated. The harmonic voltages across each component may then be calculated, and components dimensioned for the desired harmonic current absorption.

From an analysis of the equivalent circuit all relevant values can be calculated, and the impedance frequency response can be plotted as shown in Figure 8.7.

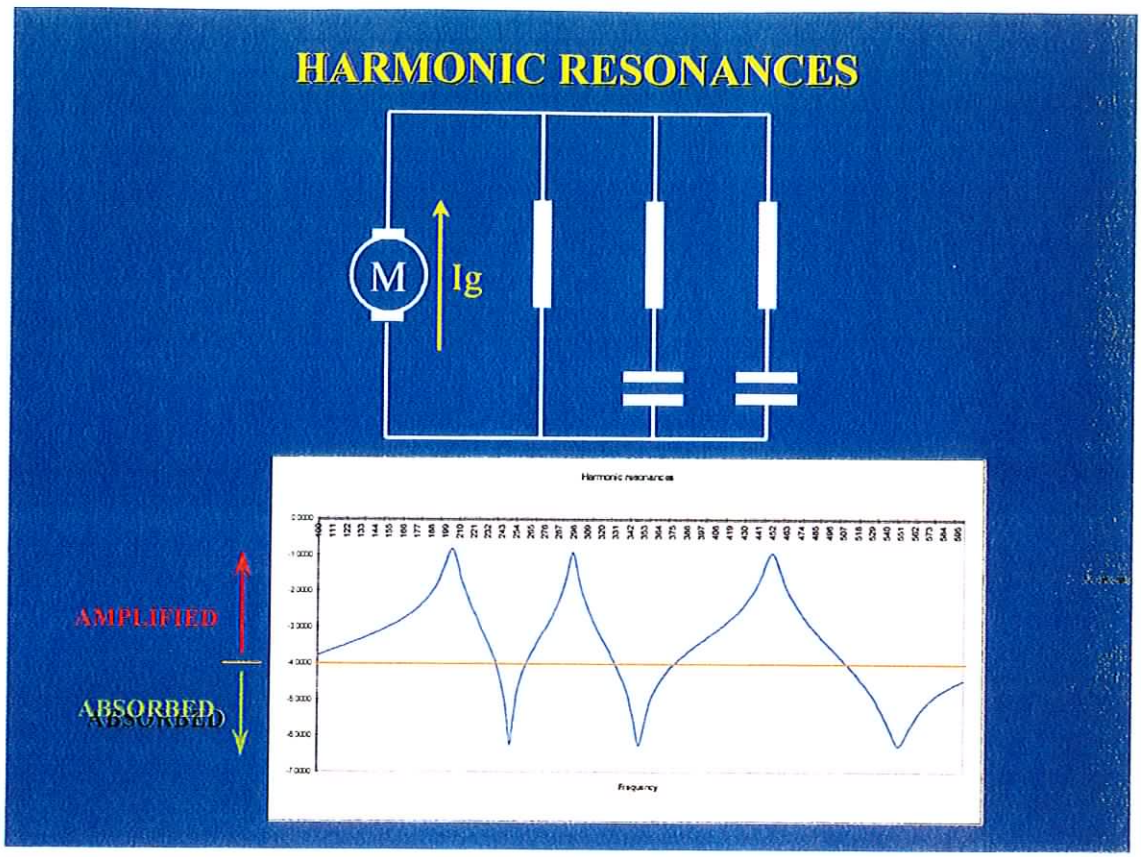


Figure 8.7 Impedance frequency response

The process of designing harmonic filter banks requires a considerable amount of calculation, because of the number of components involved, the range of component parameters to be considered and the range of frequencies covered.
For this reason the author decided to design a new programme in order to facilitate this calculation process.

8.4.2 Harmonic Filter Programme

The programme is based on an analysis of the distribution of generated harmonic currents between utility source impedance and the harmonic filter.
The programme allows the entry of:

I. Source impedance values in the form R + jX referred to the supply voltage
II. Tuning frequency for each of up to four filter branch

III. Nominal supply voltage

IV. Capacitor rated voltages for each branch

V. Capacitor rated powers at rated voltages for each branch

VI. Inductor resistance

VII. Injected harmonic current values (as measured) for harmonic numbers, 3,5,7,9,11,13,17 and 19.

The programme was designed and implemented in Microsoft Excel using its in-built complex number calculation functions (see appendix P). It consists of two Excel sheets, a data entry and a calculation sheet. Entry of up to four branches per filter bank is allowed. The calculation process is as follows:

I. Data entries (in yellow) allow the input of standard commercially available capacitor dimensions.

II. Supply system source impedance is entered.

III. The programme converts all component values to admittance.

IV. Tuning frequency is chosen by the operator.

V. The corresponding reactor values are calculated by the programme.

VI. Harmonic current values measured are entered into the programme.

VII. The programme divides current flows in the ratio of the branch admittances.

VIII. From the current values the related voltage levels are calculated.

IX. The resulting power factor correction per branch and in total is calculated.

8.4.2.1 Programme Output

The outputs produced include

(a) Per branch

I. Amps absorbed for each of the above harmonic frequencies.

II. Total current passed by each branch.

III. Total current carrying capacity of each branch, based on the capacitor values.

IV. kVAr consumption at 50 Hz.

V. Maximum voltage stress for each capacitor, based on worst case peak co-incidence for all harmonic voltages.

(b) For the complete circuit

I. Harmonics voltage distortions, individual and total, with and without filtering.

II. Harmonic currents absorbed by the compete filter bank.

III. Harmonic currents absorbed by the supply system.

IV. Total kVAr consumption by the filter bank.

(c) In addition the programme produces a graph showing a plot of harmonic impedance so that inter-arm harmonic resonance can be identified.

8.4.3 Filter Design using Harmonic Programme

8.4.3.1 Overview

The Filter Design Programme follows a practical approach (drawn from the author's experience) which makes it suitable for the standard format of component dimensioning and harmonic profiling used by the major electrical engineering manufacturers. This includes the specification of power factor capacitors, the typical results of a harmonic survey, the supply system impedance and the normal parameters required when specifying filter reactors.

8.4.3.2 Capacitor Input

Power-factor correction capacitors are normally specified by manufacturers in terms of kVAr (or MVAr) at their rated voltage. The rated voltage may be higher than the operating voltage of the system to which they are connected and so the latter value is also needed. The programme therefore allows the entry of Operating Voltage, Capacitor Voltage and Capacitor Power (at Capacitor Voltage). All of these values refer to 50 Hz.

8.4.3.3 Harmonic Measurement Input

Harmonic surveys for the purposes of designing filters normally concentrate on measuring the maximum harmonic current injected by the load into the supply system. This is normally carried out with all existing power factor correction switched off, so as not to amplify the background levels. The maximum values are recorded for each of the

harmonic values most likely to give rise to serious problems. In practice these include the odd harmonics from 3^{rd} through to the 13^{th}. The 3^{rd}, 9^{th} and other Triplene harmonics are less common due to the lack of a neutral return path in three phase machines. The 17^{th} and 19^{th} are added to this programme, as there occasionally occur resonance problems at these frequencies. Above the 19^{th}, phase cancellation tends to take phase between sources. The programme therefore allows the input of the maximum harmonic currents generated at 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th}.

8.4.3.4 System Impedance Input

Source impedance is based on the standard medium voltage supply used in the Republic of Ireland, 10 kV. This can be changed to 20kV for the upgraded network system now being installed, or to 11kV for example for UK projects. The values to be entered are the resistive and inductive impedance in ohms referred to the supply voltage (Vs) in this case 10kV.

8.4.3.5 Reactor Output

When specifying filter reactors manufacturers normally require

I. Reactor inductance for each branch.
II. Operating voltage (Vn).
III. The capacitance to which the capacitor will be connected.
IV. The values of harmonic current to be absorbed by each filter branch.

8.4.3.6 Design Steps

I. The Process of designing the filter begins with deciding the value of power factor correction, in kVAr, to be achieved (or tolerated). A value of one quarter of this may initially be entered into each branch via the capacitor entry cells.

II. If only two or three branches are required then the total should be divided by 2 or 3 as appropriate. The branches not required may be switched off by entering a very high value, such as 1,000,000 ohms, for reactor resistance.

III. For the purposes of reactor design, a Q factor of 50 is normally assumed. Most reactor manufacturers can reasonably achieve this. An initial values of 0.01 ohms may be entered into the reactor resistance cell until this is calculated from the programme output.

IV. The first precaution to be taken during the design process is to ensure that the values for Total Branch Rating are greater than for Total Branch Amps rating of the connected capacitor. This can be achieved (a) by changing the size of capacitor or (b) by increasing the maximum voltage rating of the capacitor.

V. The second precaution is to ensure that the value of Branch Capacitor Voltage (Delta) does not exceed the Capacitor Voltage. Branch Capacitor Voltage (Delta) is calculated as the arithmetic sum of the harmonic peak voltages, on the basis that a co-incidence of peaks can result in rapid capacitor failure if this occurs.

VI. Tuned frequencies may be entered for each branch. These are generally set at a frequency sufficiently far below the harmonic frequency to allow for component tolerance. Tuning should not be allowed to go above the harmonic frequency as this may lead to amplification of distortion.

VII. Capacitor values may be changed during the design process in order to achieve the necessary level of power factor correction and the desired harmonic mitigation, without overloading any of the components.

VIII. Finally the reactor resistance is calculated based on a Q factor of 50. This is entered in the reactor resistance cells. The reactor values are read off the spreadsheet and the corresponding harmonic currents, which they will carry.

8.4.4 Component Dimensioning

During the design of the specific solution for this project the following factors were taken into account:

I. The load was running at near unity power factor, and hence the filter should generate as little wattless current as possible. To achieve this it was decided to use higher voltage capacitors than normal having lower capacitance, so as to increase the ratio of harmonic to fundamental current absorption. As 690 volt capacitors are the highest standard voltage capacitors available, these were proposed for use.

II. A four-branch filter was used in order to achieve the required harmonic reductions, because the use of higher voltage (and lower capacitance) leads to filters with a narrower bandwidth.

III. It was decided to dimension the components, based upon the highest individual harmonic current for each frequency, because the generated harmonic currents varied between phases.

IV. It was decided to use standard manufactured capacitor values and to have the reactors specifically manufactured to match these.

V. A spare capacity of 25% of the measured harmonic current was included in the design of each the filter bank.

After analysis of a range of scenarios using the Excel programme, a solution was designed using a four branch filter. The component values chosen are as set out in the following Tables 8.2 and 8.3.

Branch 1	Branch 2	Branch 3	Branch 4
Tuned 148 Hz	Tuned 248 Hz	Tuned 348 Hz	Tuned 448 Hz
Capacitor power 100kVAr at 690 V	Capacitor power 200 kVAr at 690 V	Capacitor power 400 kVAr at 690 V	Capacitor power 350 kVAr at 690 V
Inductor 1.80 mH	Inductor 0.316 mH	Inductor 0.0796 mH	Inductor 0.0535 mH

Table 8.2 Filter components

Step	1	2	3	4
UN – 50Hz	3 × 400 V	3 × 400 V	3 × 400 V	3 × 400 V
QC/kVAr/400V	33.6	67.2	134.4	117.6
P%	4.726	2.163	1.2625	0.8417
Insulation Class	T40/B	T40/B	T40/B	T40/B
I1/A	55	102	198	172
Ih/A	30	95	265	145

Table 8.3 Inductor specification

Capacitors to be manufactured to IEC 60831

Inductors to be manufactured to IEC 60289

8.4.5 Filter Construction

Filter construction consists of a separate housing for each branch, in standard industrial switchboard enclosures to IEC 60947 standard.

Each branch will consist of a series filter with the capacitor elements supplied through a reactor of value as shown in Table 8.3. In addition each branch should contain a Moulded Case Circuit Breaker (MCCB), a contactor and an overload device with close excess current protection, such as motor overload relay. This should be set to trip at the maximum current carrying capacitor of the branch.

General construction of the banks is to be as set out in appendix Q

8.4.6 Filter Installation and Commissioning

The filter is to be installed in a separate switch-room adjacent to the balancer and is to be supplied from the balancer circuit breaker.

Commissioning will involve measurement of harmonic and wattless currents flowing before and after switch-in and ensuring that all design criteria are met. It will also involve a standard set of tests carried out during the commissioning of electrical power equipment, for example Megger voltage injection and current injection testing.

8.4.7 Final Completion

The harmonic filter bank extension has been fully designed and costed. Unfortunately due to cutbacks it has not been regarded as a high priority task given that the load is operating reliably with the balancer as it stands. It is now planned to install this unit in 2003.

CHAPTER 9
CONCLUSIONS

9.1 Overview

The following objectives have been achieved:

I. New solutions have been developed, designed, installed, commissioned and tested to solve some of the major power quality problems facing industrial electricity consumers using large unbalanced and non-linear loads.

II. Two new phase-balancing systems have been developed and compared; the first using the combination of a negative phase sequence current generating pilot motor and capacitor/inductor steps; the second using capacitor/inductor steps only and an idling motor.

III. A full-sized version of each type of phase-balancing systems has been constructed and installed at the Waterford Crystal plants in Kilbarry and Dungarvan, County Waterford, Ireland. It has been shown that the capacitor/inductor type facilitates repeatability in design and construction.

IV. A new harmonic filter bank calculation programme and design system has been developed. The design procedure facilitates repeatability in design and construction of harmonic filter banks.

9.2 Balancers compared

The two balancing systems are functioning successfully and to the satisfaction of the client. However there is a significant difference in the practicality of the designs. While it is possible to design and build a balancer using a pilot motor to generate negative phase sequence current, this would be difficult to repeat economically in standard production, due to the effect of minor changes in the motor parameters, as already mentioned in section 5.4.4.

Each pilot motor balancer would require the separate testing of all motors and the likelihood of considerable time being spent in the individual tuning of the balancer once connected to the load. Compared to this the construction of a capacitor/inductor balancer is very straightforward once it has been properly designed. The latter is also considerably more flexible in use. Steps can easily be moved between phase pairs as the connected load is changed.

With the capacitor/inductor balancer it is relatively easy to build a unit with many automatically switched steps in order to follow a given load profile. To achieve this with the pilot motor method would require the construction of suitable motorised Variac units in order to change the amount of negative phase sequence current generated by the balancer as the load varied. The design construction and control of such a balancer would be a challenging and costly undertaking when compared to the capacitor/inductor method.

9.3 Harmonic filter design

A new harmonic filter bank calculation programme and design system has been developed. This filter design system allows the entry and comparison of standard specifications and values, as used by the power factor correction industry. It provides all of the parameters required to specify the components needed to construct a filter of up to four branches, each having a different tuned frequency. Three tuned frequencies are the maximum number normally required in practice, with four being used on very rare occasions.

A filter bank has been designed to mitigate the harmonic distortion experienced at the glass furnace at Waterford Crystal, Dungarvan, Ireland. A detailed design for this bank is described. It is proposed to construct and install this unit during 2003.

9.4 Future Research

In theory it would be possible to design and construct a balancer consisting of three separate modules one for each phase pair, which could follow any level of unbalance across the three phases. This could form the subject of a separate research project.

It is also suggested that the replacement of the idling motors in the capacitor/inductor balancing system be examined. Another suitable voltage dependent impedance may be found which could replace these, at a lower cost and with lower running losses.

Appendices

Appendix A Balancer Programme

(written in C++)

```
/*   balancer programme declarations */

#include <conio.h>
#include <stdio.h>
#include <complex.h>


double rt3_2 = (sqrt(3))/2 ; /* for root 3 over 2 */
complex  a = complex ( -0.5 , rt3_2 ); /*alpha*/
complex  a2 = complex ( -0.5 , - rt3_2); /*alpha squared*/

int  VRSFLAG,VSTFLAG,VTRFLAG,AFLAG ;
int  BFLAG,Z1PFLAG,Z2PFLAG,XLFLAG ;
int  XCFLAG,ZLFLAG,ZSFLAG,CHX,CHFLAG,GOFLAG;
int  i, flag, x,y, z, n;
int  sign_cnt,j_cnt,dp_cnt,j;

double AV,BV,A,B,I11_mag,I21_mag,r_part,j_part,mag_V11,mag_V21,NPS1,NPS2,
          IR_mag,IS_mag,IT_mag,ITP_mag,IRP_mag,ISP_mag,V2P_mag,IRR,ISS,ITT,
          I_AV_section,KVA_AV_section,I_middle_section,KVA_middle_section,
          I_BV_section,KVA_BV_section,X;

complex  XL,XC,VRS,VST,VTR,A1,A2,A3,A4,B1,B2,B3,B4;
complex  Z1P,Z2P, XS, Y1P,Y2P,ZS,ZL,I11,I21;
complex  V1P,V2P,IRP,ISP,ITP,IR,IS,IT,I1P,I2P;
complex VR1S1,VS1T1,VT1R1,V11,V21;

char string[50], r_string[50], j_string[50];
char  c,*ch,hh;
char buffer[50];
char msg[100];
```

```
void calculate_balancer_details()
/* This is the main balancer calculation subroutine */

{
V1P = (VRS/A2- VTR/A4)/(A1/A2-A3/A4);
/*Pilot motor terminal V pos phase seq*/

V2P = VRS/A2 - A1/A2*V1P;
/*Pilot motor terminal V neg phase seq*/

IR=((1+a2*AV+BV)*Y1P–((a–1)+BV*(1–a2)/(1–AV+BV))/XL
        +((1–a2)/(1–AV+BV))/ZL)*V1P
        +((1+a*AV+BV)*Y2P–((a2–1)+BV*(1–a)/(1–AV+BV))/XL
        +((1–a)/(1–AV+BV))/ZL)*V2P
/*line current -- load and balancer (complex)*/

IS=((a2–a2*AV–BV)*Y1P+((a2–a)–AV*(1–a2)/(1–AV+BV))/XC
        –((1–a2)/(1–AV+BV))/ZL)*V1P
        +((a–a*AV–BV)*Y2P+((a–a2)–AV*(1–a)/(1–AV+BV))/XC
        –((1–a)/(1–AV+BV))/ZL)*V2P
         /*line current -- load and balancer (complex)*/

IT=(a*Y1P+((a–1)+BV*(1–a2)/(1–AV+BV))/XL
        –    ((a2–a)–AV*(1–a2)/(1–AV+BV))/XC)*V1P
        +(a2*Y2P+((a2–1)+BV(1–a)/(1–AV+BV))/XL
        –((a–a2)–AV(1–a)/(1–AV+BV))/XC)*V2P
          /*line current -- load and balancer (complex)*/

IR_mag =  sqrt(norm(IR));  /*line current magnitude (load and balancer)*/
IS_mag =  sqrt(norm(IS));  /*line current magnitude (load and balancer)*/
IT_mag =  sqrt(norm(IT));  /*line current magnitude (load and balancer)*/

I1P = Y1P*V1P; /*Pilot motor current -- pos phase seq*/
I2P = Y2P*V2P; /*Pilot motor current -- neg phase seq*/

IRP = I1P+I2P;        /*Pilot motor current (complex)*/
ISP = a2*I1P + a*I2P;  /*Pilot motor current (complex)*/
ITP = a*I1P + a2*I2P;  /*Pilot motor current (complex)*/

IRP_mag = sqrt(norm(IRP)); /*Pilot motor current (magnitude)*/
ISP_mag = sqrt(norm(ISP)); /*Pilot motor current (magnitude)*/
ITP_mag = sqrt(norm(ITP)); /*Pilot motor current (magnitude)*/

I11 = ((IT-IR) -a2*(IR-IS))/3/a; /*system current pos phase seq component*/
I21 = ((IT-IR) -a*(IR-IS))/3/a;  /*system current neg phase seq component*/

I11_mag =  sqrt(norm(I11));    /* system current magnitude PPS component*/
I21_mag =  sqrt(norm(I21));    /* system current magnitude NPS component*/



X = real(IR);X = sqrt( pow(X,2));
IRR  =  X /IR_mag;          /* System current power factor R phase*/

X = real(IS);sqrt( pow(X,2));
ISS  =  X /IS_mag;          /* System current power factor S phase*/

X = real(IT);sqrt( pow(X,2));
ITT  =  X /IT_mag;          /* System current power factor T phase*/
```

```
/*Auto-transformer currents and KVA rating calculations*/

I_AV_section = ((1-AV)*ISP_mag-BV* IRP_mag); /*current in AV section*/
KVA_AV_section = AV*((1-AV)*ISP_mag-BV* IRP_mag); /*KVA in AV section*/

I_middle_section = (AV*ISP_mag+BV* IRP_mag); /*current in middle section*/
KVA_middle_section = (1-AV)*(AV*ISP_mag+BV* IRP_mag); /*KVA in middle section*/

I_BV_section = IRP_mag; /*current in BV section*/
KVA_BV_section = BV*I_BV_section; /*KVA in BV section*/

}
```

```
void negative_phase_sequence(void)
/* From the voltage results this subroutine calculates the
        percentage negative phase sequence at the load and balancer terminals */

{
VR1S1 = VRS + ZS*(IS - IR);   /*     Phase voltages     */
        VS1T1 = VST + ZS*(IT - IS);   /*      at R1,S1,         */
        VT1R1 = VTR + ZS*(IR - IT);   /*     and T1 points      */
        V11 = (VT1R1 -a2*VR1S1)/3/a;  /*     V PPS of above     */
        V21 = ( VT1R1 -a*VR1S1)/3/a;  /*     V NPS of above     */
        mag_V11 = sqrt(norm(V11));    /*    magnitude of V PPS    */
        mag_V21 = sqrt(norm(V21));    /*    magnitude of V NPS    */
        NPS1 = mag_V21/mag_V11*100;   /* percentage V NPS at load */
}
```

```
/* These subroutines calculate A1, A2, A3 and A4. */

void  calculate_A1()
{
A1 = ((1+2*a2*AV-a2+2*BV)*Y1P
          + 2/(1-AV+BV)*(1-a2)/ZL
          - 1/XL*((a-1) + BV/(1-AV+BV)*(1-a2))
          - 1/XC*((a2-a)  - AV/(1-AV+BV)*(1-a2)))*ZS
          + (1-a2)/(1-AV+BV);
}


void  calculate_A2()
{
A2 = ((1-a+2*a*AV+2*BV)*Y2P
          + 2/(1-AV+BV)*(1-a)/ZL
          - 1/XL*((a2-1) + BV/(1-AV+BV)*(1-a))
          - 1/XC*((a-a2) - AV/(1-AV+BV)*(1-a2)))*ZS
          + (1-a)/(1-AV+BV);
}


void  calculate_A3()
{
A3 = ((a-1-a2*AV-BV)*Y1P
          + 2/XL*((a-1) + BV/(1-AV+BV)*(1-a2))
          - 1/XC*((a2-a) - AV/(1-AV+BV)*(1-a2))
          - 1/(1-AV+BV)*(1-a2)/ZL)*ZS
          + (a-1)
          +  BV/(1-AV+BV)*(1-a2);
}


void  calculate_A4()
                    {
A4 = ((a2-1-a*AV-BV)*Y2P
          + 2/XL*((a2-1) + BV/(1-AV+BV)*(1-a))
          - 1/XC*((a-a2) - AV/(1-AV+BV)*(1-a))
          - 1/(1-AV+BV)*(1-a)/ZL )*ZS
          + (a2-1)
          +  BV/(1-AV+BV)*(1-a);
          }
```

```
void  calc_T_voltage()
    /* This subroutine calculated the T voltage with T phase removed
          and R & S connected */

{
          B1 = (1-a2)/(1-AV+BV);
          B2 = (1-a)/(1-AV+BV);
                    B3 = (a-1)+(BV*(1-a2)/(1-AV+BV));
          B4 = (a2-1)+(BV*(1-a)/(1-AV+BV));

          V1PT = (-a2*Y2P/B2-(1+B4/B2)*1/XC-(B4/B2)*1/XL)/
                              (a*Y1P+a2*Y2P*B1/B2+(B3-B4*B1/B2)/XC
                                        +(B3-B4*B1/B2)/XL)*VRS;
          /* V1PT is pilot motor V1 with T removed */
          V2PT = (VRS-B1*V1PT)/B2;
          /* V2PT is pilot motor V2 with T removed */
          VTRT = B3*V1PT+B4*V2PT;
          VSTT = -VRS-VTRT;
          /* VTRT and VSTT are the Vtr and Vst with T removed */
          VTRT_mag =  sqrt(norm(VTRT));
          VSTT_mag =  sqrt(norm(VSTT));   /*needs to be checked*/
}



void  calculate_all(void)
/* This subroutine calculates all the main values */

{
          calculate_A1();
          calculate_A2();
          calculate_A3();
          calculate_A4();
          calculate_balancer_details();
          negative_phase_sequence();
}



void find_best_AB(void)
/* This subroutine iterates through all possible A and B values to find the one giving
          the minimum negative phase sequence voltage */

{
          NPS2=100;
          for(AV=0;AV<1.00;AV =AV+.01)
                    {
                    for(BV=0;BV<1.00;BV =BV+.01)
                              {
                              calculate_all();
                              if (NPS1<NPS2)
                                        {
                                                  NPS2=NPS1;
                                                  A=AV;
                                                  B=BV;
                                        }
                              } /*end for BV*/
                    } /*end for AV*/
}/*End find_best_AB*/
```

```
void  final_calculation_with_best_AB(void)

/* This subroutine does the final calculations on the best A and B values, calculates
        the T voltage and prints the results */
{
        AV = A;
        BV = B;
        calculate_all();
        calc_T_voltage();
        results_print();
}




void results_print(void);

/* This subroutine prints all required results */

{
printf( " System voltage  = %.2f %\n\n",VRS_mag);
printf( " Load terminal voltage =  ",VR1S1_mag);printf("","\n");
printf( " XL = ",XL);printf("","\n");
printf( " XC = ",XC);printf("","\n");
printf( " Motor Z1 'ohms' = ", Z1P);printf("","\n");
printf( " Motor Z2 'ohms' = ", Z2P);printf("","\n");
printf( " System impedance (ohms) = ", ZS);printf("","\n");
printf( " Load impedance (ohms) = ", ZL);printf("","\n");
printf( " A = ", A);
printf( "       B = ", B);printf("","\n");
printf( " Pilot motor Amps, Ir = ", IRP_mag);
printf ( ",  Is = ", ISP_mag);
printf ( ",  It = ", ITP_mag);printf( "" , "\n");
printf ( " Load and balancer total IR Amps = ", IR_mag);
printf ( "  at power factor  ", IRR);printf( "" , "\n");
printf ( " Load and balancer total IS Amps = ", IS_mag);
printf ( "  at power factor  ", ISS);printf( "" , "\n");
printf ( " Load and balancer total IT Amps = ", IT_mag);
printf ( "  at power factor  ", ITT);printf( "" , "\n");
printf ( " Negative phase sequence voltage =    ", NPS1);
printf( "" , "\n");
printf ( " Auto-transformer current AV section ", I_AV_section);printf( "" , "\n");
printf ( " Auto-transformer KVA in AV section ", KVA_AV_section);printf( "" , "\n");
printf ( " Auto-transformer current mid section = ", I_middle_section);printf( "" , "\n");
printf ( " Auto-transformer KVA in middle section = ", KVA_middle_section);
printf( "" , "\n");
printf ( " Auto-transformer current BV section = ", I_BV_section);printf( "" , "\n");
printf ( " Auto-transformer KVA in BV section ", KVA_BV_section);printf( "" , "\n");
printf ( " Capacitor voltage with T phase removed = ", VSTT_mag);
printf ( " Inductor voltage with T phase removed = ", VTRT_mag);
}
```

```
void main(void)

/* This is the main programme */

{

        textmode(C80);
        textbackground(BLUE);
        textcolor(YELLOW);


        VRSFLAG = 0; VSTFLAG = 0;   VTRFLAG =  0;   AFLAG = 0;
        BFLAG = 0;  Z1PFLAG = 0;   Z2PFLAG =0;   XLFLAG = 0;
        XCFLAG = 0; ZLFLAG = 0;   ZSFLAG = 0;  CHX =0,CHFLAG = 0;

        NPS2 = 100; /* set maximum initial percentage NPS voltage*/

        do
        {
                CHFLAG = 0;
                clrscr();
                enter_data();
                clrscr();
                checkdat ();
        }while ( CHFLAG == 1 );

        calculate_all();
        final_calculation_with_best_AB()

        do
        {
                cout << " Go again?       Yes =  Space_bar / No = any other key :";
                GOFLAG = 0;
                hh = getche()  ;
                if ( hh == 32)
                {
                do
                {
                        CHFLAG = 0;
                        clrscr();
                 enter_data();
                        clrscr();
                        checkdat ();
                }
                while ( CHFLAG == 1 );
        GOFLAG = 1;
        calculate_all();
        }
        }while ( GOFLAG == 1 ) ;
         final_calculation_with_best_AB()
} /*End main routine*/
```

```
void enter_data()
/* This subroutine allows the entry of all necessary data */

{
        clrscr();
        if( VRSFLAG == 0)
        {
                cout << " Enter VRS A + jB :   VRS =>";
                get_parts();
                VRS= complex(r_part,j_part);
                cout <<"\n"<< "Enter system VRS = " << VRS <<  " Volts"  << " \n\n";
                VST= VRS*a2;
                cout <<"\n"<< "          VST = " << VST <<  " Volts"  << " \n\n";
                VTR= VRS*a;
                cout <<"\n"<< "          VTR = " << VTR <<  " Volts"  << " \n\n";
        }



        if(XLFLAG == 0)
        {
                cout << " Enter XL   =>";
                get_parts();cout << " Ohms";
                XL = complex(r_part,j_part);
                cout <<"\n"<< "       XL = " << XL <<  " "  << " \n\n";
        }


        if(XCFLAG == 0)
        {
                cout << " Enter XC   =>";
                get_parts();cout << " Ohms";
                XC= complex(r_part,j_part);
                cout <<"\n"<< "       XC = " << XC <<  " "  << " \n\n";
        }


        if(Z1PFLAG == 0)
        {
                cout << " Enter  Motor Z1:  R1P + j X1P  => ";
                get_parts();
                Z1P = complex(r_part,j_part);
                Y1P = 1/Z1P;
                cout <<"\n"<< "          Y1P = " << Y1P <<  " Mhos"  << " \n\n";
        }


        if(Z2PFLAG == 0)
        {
                cout << " Enter  Motor Z2:  R2P + j X2P  => ";
                get_parts();
                Z2P= complex(r_part,j_part);
                Y2P = 1/ Z2P;
                cout <<"\n"<< "          Y2P = " << Y2P <<  " Mhos"  << " \n\n";
        }
```

```
        if(ZSFLAG == 0)
        {
                cout << " Enter  System Impedance, ZS:   RS + j XS  => ";
                get_parts();
                ZS = complex(r_part,j_part);
                cout <<"\n"<< "              ZS = " << ZS <<  " Ohms"  << " \n\n";
        }


        if(ZLFLAG == 0)
        {
                cout << " Enter  Load Impedance, ZL:   RL + j XL  => ";
                get_parts();
                ZL = complex(r_part,j_part);
                cout <<"\n"<< "              ZL = " << ZL <<  " Ohms"  << " \n\n";
                CHFLAG = 0 ;
        }

} /*End void enter_data()*/
```

```
void checkdat()
/* This subroutine allows all entered data to be checked and changed */

{
        cout << " Is this the Input Data required ? Y to verify, Space to cancel.  "<< "\n" ;
        cout <<"\n"<< "          VRS = " << VRS <<  " Volts" << "\n"  ;
        cout << "              Change This Data ? Y/N ";
        do
                {
                        CHX = 0;
                        hh = getch();
                        if ( hh == 89) hh = 121;
                        if ( hh  == 121 )
                        {
                                VRSFLAG = 0;
                                CHFLAG = 1;
                                CHX = 1;
                                cout << "Yes";
                        }
                if ( hh ==  32 )
                {
                        CHX = 1  ;
                        VRSFLAG = 1;
                        cout << "No";
                }
        }while( CHX != 1);


        cout <<"\n"<< "          VST = " << VST <<  " Volts"<< "\n"  ;
        cout << "              Change This Data ? Y/N ";
        do
        {
                CHX = 0;
                hh = getch();
                if ( hh == 89) hh = 121;
                if ( hh  == 121 )
                {
                        VSTFLAG = 0;
                        CHFLAG = 1;
                        CHX = 1;
                        cout << "Yes";
                }
                if ( hh ==  32 )
                {
                        CHX = 1  ;
                        VSTFLAG = 1;
                        cout <<"No";
                }
        }while( CHX != 1);
```

```
cout <<"\n"<< "          VTR = " << VTR <<  " Volts"<<  "\n"   ;
cout << "              Change This Data ? Y/N ";
do
        {
                CHX = 0;
                hh = getch();
                if ( hh == 89) hh = 121;
                if ( hh  == 121 )
                {
                        VTRFLAG = 0;
                        CHFLAG = 1;
                        CHX = 1;
                        cout <<" Yes";
                }
                if ( hh ==  32 )
                {
                        CHX = 1  ;
                        VTRFLAG = 1;
                        cout << "No";
                }
        }while( CHX != 1);


cout <<"\n"<< "          XL = " << XL << "\n"   ;
cout << "              Change This Data ? Y/N ";
do
        {
                CHX = 0;
                        hh = getche();
                        if ( hh == 89) hh = 121;
                        if ( hh  == 121 )
                        {
                                XLFLAG = 0;
                                CHFLAG = 1;
                                CHX = 1;
                                cout << " Yes";
                        }
                        if ( hh ==  32 )
                        {
                                CHX = 1  ;
                                XLFLAG = 1;
                                cout << " No";
                        }
        }while( CHX != 1);
```

```
cout <<"\n"<< "          XC = " << XC << "\n" ;
cout << "              Change This Data ? Y/N ";
do
        {
                CHX = 0;
                hh = getche();
                if ( hh == 89) hh = 121;
                if ( hh  == 121 )
                {
                        XCFLAG = 0;
                        CHFLAG = 1;
                        CHX = 1;
                        cout << " Yes";
                }
                if ( hh ==  32 )
                {
                        CHX = 1;
                        XCFLAG = 1;
                        cout << "No";
                }
        }while( CHX != 1);


cout <<"\n"<< "          Z1P = " << Z1P <<  " Ohms" << "\n" ;
cout << "              Change This Data ? Y/N ";
do
        {
                CHX = 0;
                hh = getche();
                if ( hh == 89) hh = 121;
                if ( hh  == 121 )
                {
                        Z1PFLAG = 0;
                        CHFLAG = 1;
                        CHX = 1;
                        cout << " Yes";
                }
                if ( hh ==  32 )
                {
                        CHX = 1  ;
                        Z1PFLAG = 1;
                        cout << "No";
                }
        }while( CHX != 1);
```

```
cout <<"\n"<< "          Z2P = " << Z2P <<  " Ohms" << "\n"  ;
cout << "              Change This Data ? Y/N ";
do
        {
                CHX = 0;
                hh = getche();
                if ( hh == 89) hh = 121;
                if ( hh  == 121 )
                {
                        Z2PFLAG = 0;
                        CHFLAG = 1;
                        CHX = 1;
                        cout << " Yes";;
                }
                if ( hh ==  32 )
                {
                        CHX = 1  ;
                        Z2PFLAG = 1;
                        cout << " No";
                }
        }while( CHX != 1);


cout <<"\n"<< "          ZS = " << ZS <<  " Ohms" << "\n"  ;
cout << "              Change This Data ? Y/N ";
do
        {
                CHX = 0;
                hh = getche();
                if ( hh == 89) hh = 121;
                if ( hh  == 121 )
                {
                        ZSFLAG = 0;
                        CHFLAG = 1;
                        CHX = 1;
                        cout << " Yes";
                }
                if ( hh ==  32 )
                {
                        CHX = 1  ;
                ZSFLAG = 1;
                cout << " No";
                }
        }while( CHX != 1);
```

```
cout <<"\n"<< "          ZL = " << ZL <<  " Ohms"  << "\n" ;
cout << "              Change This Data ? Y/N ";
do
        {
                CHX = 0;
                hh = getche();
                if ( hh == 89) hh = 121;
                if ( hh  == 121 )
                {
                        ZLFLAG = 0;
                        CHFLAG = 1;
                        CHX = 1;
                        cout << " Yes";
                }
                if ( hh ==  32 )
                {
                        CHX = 1  ;
                        ZLFLAG = 1;
                        cout << "No";
                }
        }while( CHX != 1);

} /*End checkdat()*/
```

```
double get_parts()

/* This subroutine gets real and imaginary input components and traps input errors */

{
        do  /*while( flag == 1)*/
        {
                for( n = 2 ; n<= 50; n++)
                {
                        buffer[n] = 0;      /* clear buffers and strings. */
                        r_string[n-2] = 0;
                        j_string[n-2] = 0;
                }

        I       f ( flag == 1)
                {
                        for( n = 1; n <= buffer[1]-1; n++) printf( "\b%c\b", 00);
                        flag = 0;    /* reset flag */
                }

                dp_cnt =0;
                sign_cnt = 0;
                j_cnt = 0, j = 0, z = 0;
                buffer[0] = 50 ;       /* Get Complex Number in form */
                ch = cgets( buffer);   /*  a + j b  as char. String  */
                                       /* may include spaces.        */
                x  =  2; /* set values for scanning buffer */
                y =  0;

                do {
                        c = buffer[x];  /* scan buffer*/
                        if ( c == 32 )  /* trap SPACE char */
                        {
                                x--;
                                y++;
                                for (  n = ( x+1) ; n <= (buffer[1] +3 - y )  ; n++)
                                {
                                buffer[n] = buffer[n+1]; /* move array back one space */
                                }                        /* skipping allowed chars. */
                        }
                                x++;
                    } while ( buffer[x-2] |= 0 );  /* until  reach end of buffer */


                buffer[1] = x-4; /* new no. of characters */

                if( buffer[2] != 43  && buffer[2] != 45 )
                {
                        for( n = buffer[1]+2; n >= 1; n--) buffer[n+1] = buffer[n];
                        buffer[2] = 43;
                        buffer[1] = buffer[1]+1; /* adds + to start of string if none */
                }
```

```
flag = 0;   /* set flags to indicate if string includes */
            /* undesirable characters! */
if ( buffer[2] != 0 && buffer[1] == 0  )
            flag = 1;
/* trap RETURN as first entry */

for ( i = 2 ; i <= buffer[1]+2; i++) /* scan new buffer */
            {
            c = buffer[i];
            if(  c == 106 ) j = i; /* get j */
            }
            z = j;

if( j > 3 )
j = 4;  /* limit j to 4 for switch */

if( z > 0)
            {
            if(   buffer[z-1] != 43 && buffer[z-1] != 45 ) j = 1 ;
            }                              /* trap no sign before j */

switch (j)
{
 case 1: flag = 1 ;
break;


case 0:    x = buffer[1]; x=x+1;
if  (( buffer[x]) == 43 ||( buffer[x]) == 45 ||
     ( buffer[x]) == 46 ||( buffer[x]) == 106 )
            {
                        flag = 1;
                        break; /* END */
            }

for( n = 2; n <= x; n++)
            {
            c = buffer[n];      /* fill r_string */
            r_string[n-2] = c;
            if( c  == 44 || c == 47 || c < 43 ||  c > 57)  flag =  1;
            if( c == 43 || c == 45 ) sign_cnt++;
            if( c == 46 ) dp_cnt++;
            if( c == 106 ) j_cnt++;
            }


 if( sign_cnt > 1 || dp_cnt > 1  ) flag = 1;
 r_part = atof( r_string); j_part = 0 ;
break;  /* END */
```

```
case 3:
        buffer[3] = buffer[2]; /* put sign in j  location */
        x = buffer[1]; x=x+1;  /* last location */
        if  (( buffer[x]) == 43 ||( buffer[x]) == 45 ||
           ( buffer[x]) == 46 ||( buffer[x]) == 106 )
                {
                flag = 1;      /* +, -, .,j in last location */
                break;
                }

        for( n = 3; n <= x; n++)
        {
                c = buffer[n];       /* fill j_string */
                j_string[n-3] = c;
                if( c  == 44 || c == 47 || c < 43 ||  c > 57 ) flag=1;
                if( c == 43 || c == 45 ) sign_cnt++;
                if( c == 46 ) dp_cnt++;
                if( c == 106 ) j_cnt++;
        }

        if( sign_cnt > 1 || dp_cnt > 1  ) flag = 1;
        j_part = atof( j_string);
        r_part = 0 ;
break;  /* END */
```

```
                case 4:
                        for( n = 2; n <= z-2; n++)
                        {
                                c = buffer[n];
                                r_string[n-2] = c;
                                if( c  == 44 || c == 47 || c < 43 ||  c > 57)  flag =  1;
                                if( c == 43 || c == 45 ) sign_cnt++;
                                if( c == 46 ) dp_cnt++;
                                if( c == 106 ) j_cnt++;
                        }

                        if( sign_cnt > 1 || dp_cnt > 1  ) flag = 1;
                        r_part = atof( r_string);
                        dp_cnt = 0;
                        sign_cnt = 0;
                        j_cnt = 0 ; /* re-set */
                        buffer[z] = buffer[z-1]; /* put sign in j  location */
                        x = buffer[1]; x=x+1;  /* last location */


                        if  (( buffer[x]) == 43 ||( buffer[x]) == 45 ||
                            ( buffer[x]) == 46 ||( buffer[x]) == 106 )
                        {
                                flag = 1;
                                break;
                        }          /* +, -, .,j in last location */

                        for( n = z; n <= x; n++)
                        {
                                c = buffer[n];
                                j_string[n-z] = c;
                                if( c  == 44 || c == 47 || c < 43 ||  c > 57 ) flag=1;
                                if( c == 43 || c == 45 ) sign_cnt++;
                                if( c == 46 ) dp_cnt++;
                                if( c == 106 ) j_cnt++;
                        }

                        if( sign_cnt > 1 || dp_cnt > 1  ) flag = 1;
                        j_part = atof( j_string);
                break;
                } /* End switch (j) BREAK POINT */


        }while( flag == 1);   /*end do*/

        return r_part,j_part;


}   /*end double get_parts()*/
```

Appendix B Balancer Programme Results

System voltage = 400
Load terminal voltage = 397.174
XL = (0, 1.6)
XC = (0, - 1.6)
Motor Z1 'ohms' = (0.066, 1.83)
Motor Z2 'ohms' = (.031, 0.15)
System impedance (ohms) = (0.00139, 0.00733)
Load impedance (ohms) = (0.53333, -0)

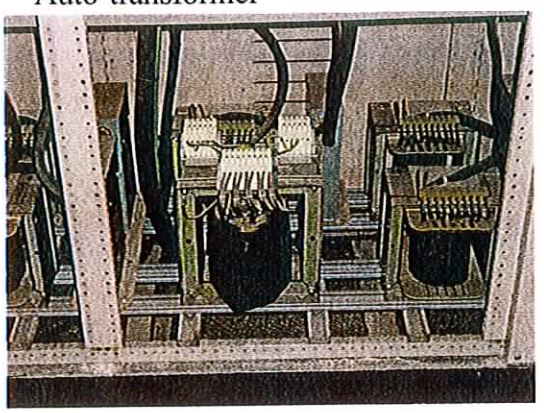
A = 0.225, B = 0.155
Pilot motor Amps, Ir = 272.749, Is = 63.9755, It = 234.632
Load and balancer total IR Amps = 458.609, at power factor 0.950579
Load and balancer total IS Amps = 460.204, at power factor 0.950337
Load and balancer total IT Amps = 459.1, at power factor 0.949519
Negative phase sequence voltage % = 0.00306933

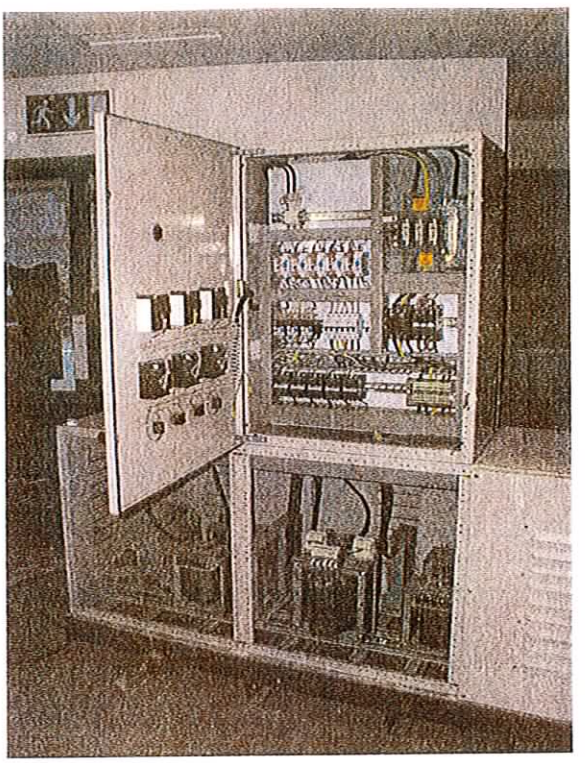
Auto-transformer current AV section = 49.581
Auto-transformer KVA in AV section = 11.1557
Auto-transformer current mid section = 56.6706
Auto-transformer KVA in middle section = 43.9197
Auto-transformer current BV section = 272.749
Auto-transformer KVA in BV section = 42.2761

Capacitor voltage with T phase removed = 473.603
Inductor voltage with T phase removed = 295.324

Appendix C Photographs of Prototype Balancer

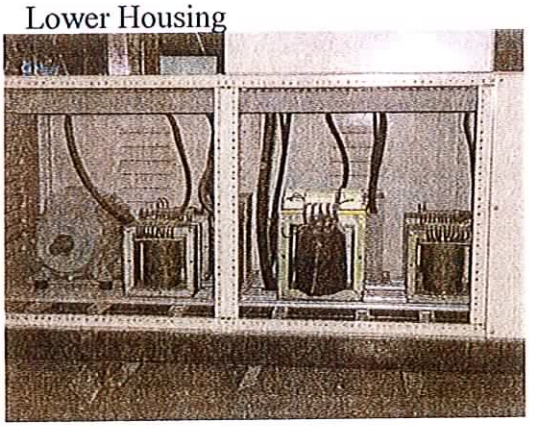
Auto-transformer



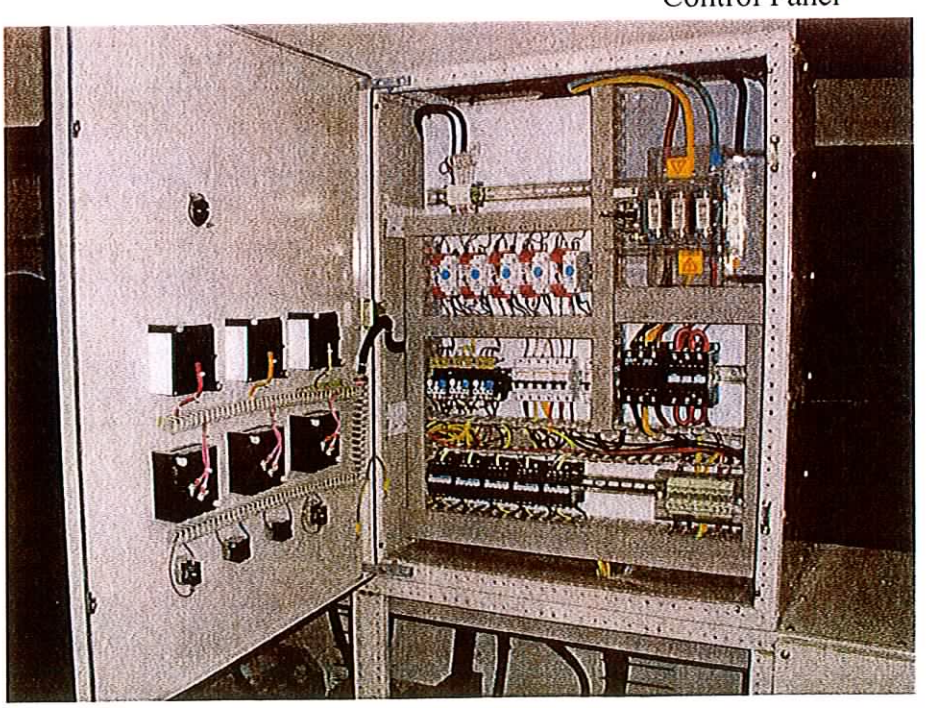


Balancer Assembly

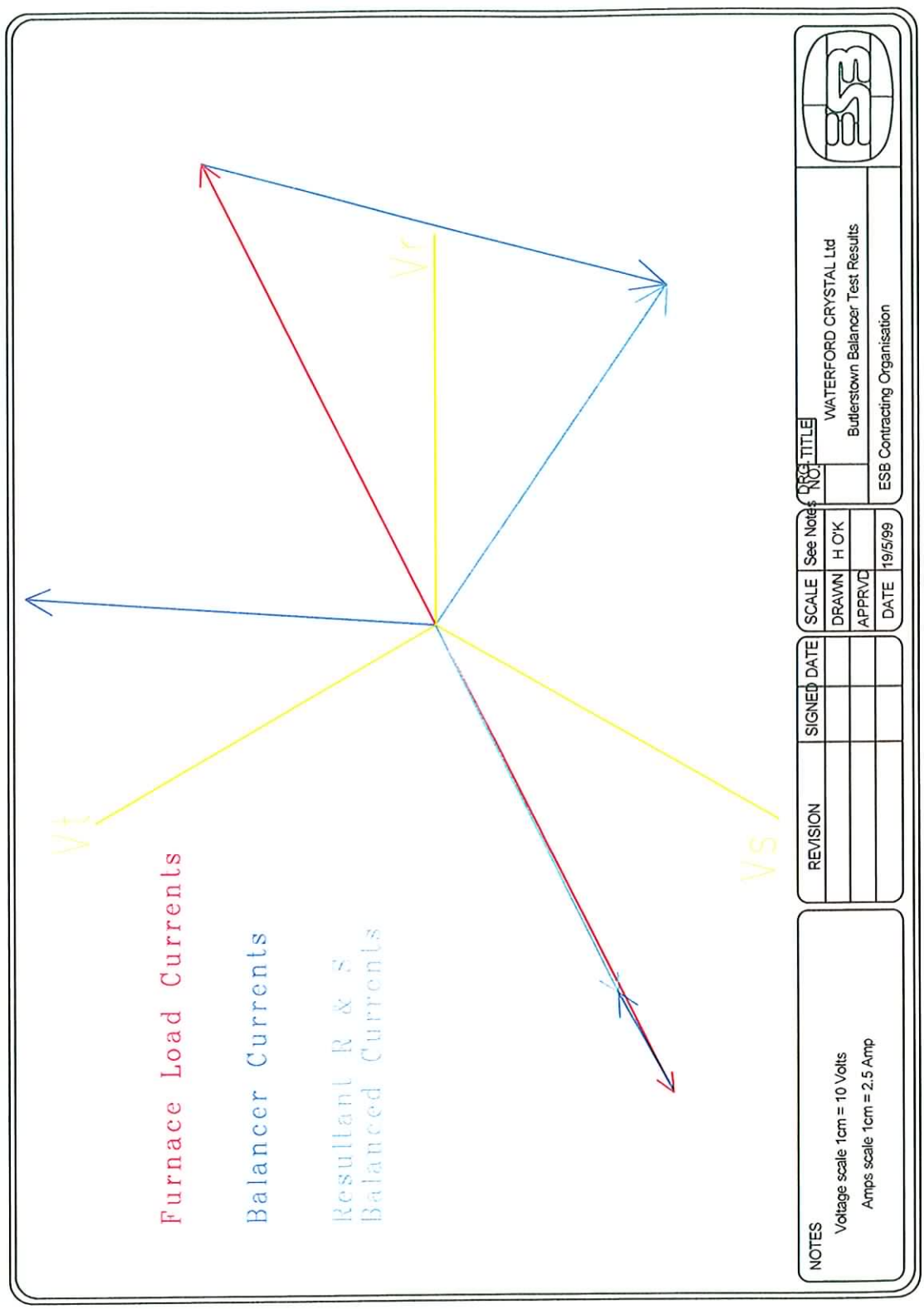
Lower Housing



Control Panel

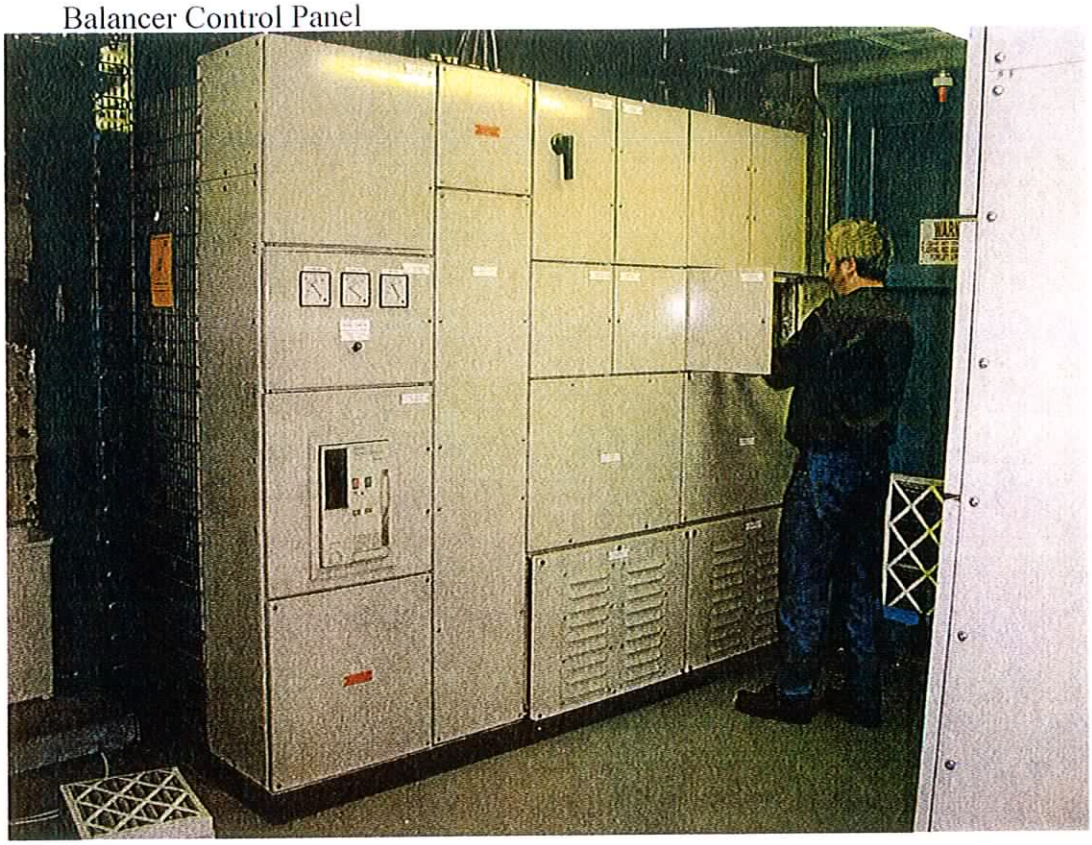


Appendix D Prototype Balancer Test Results

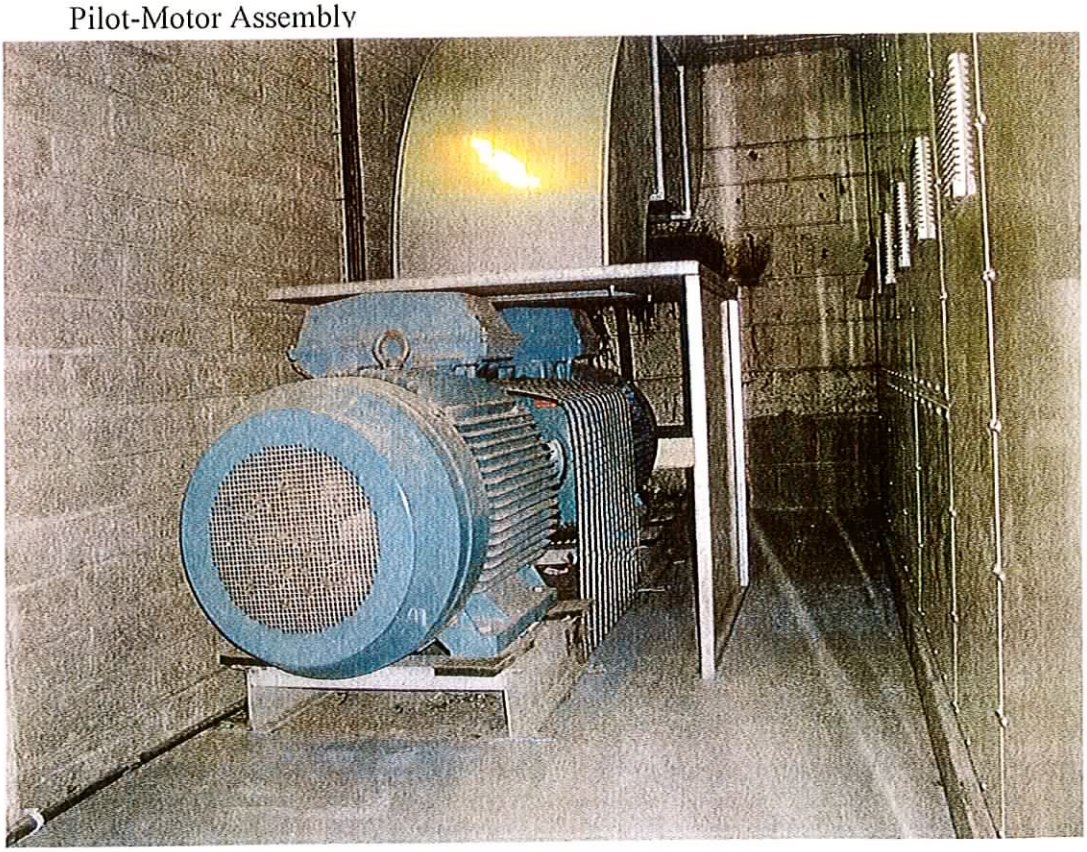


Appendix E Photographs of Production Balancer

Balancer Control Panel



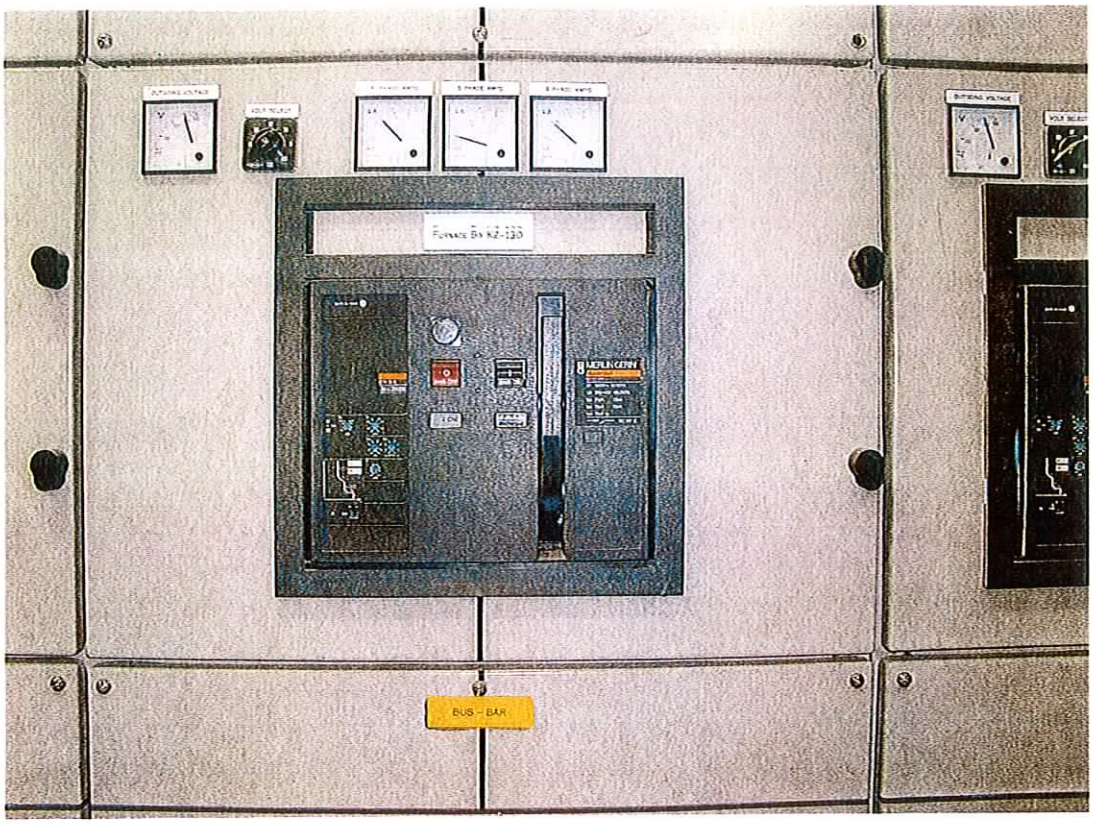
Pilot-Motor Assembly



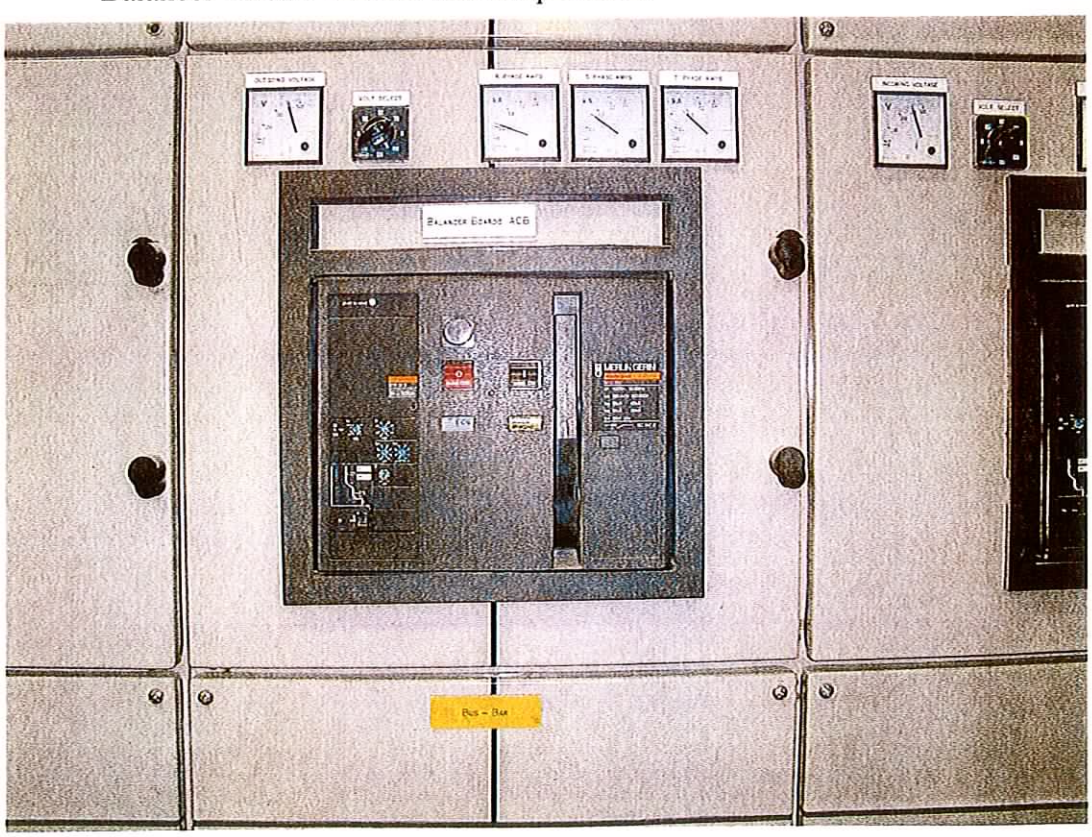
Auto-Transformers

Furnace Main-Switchboard

Furnace Circuit-Breaker and Amp-Meters



Balancer Circuit-Breaker and Amp-Meters

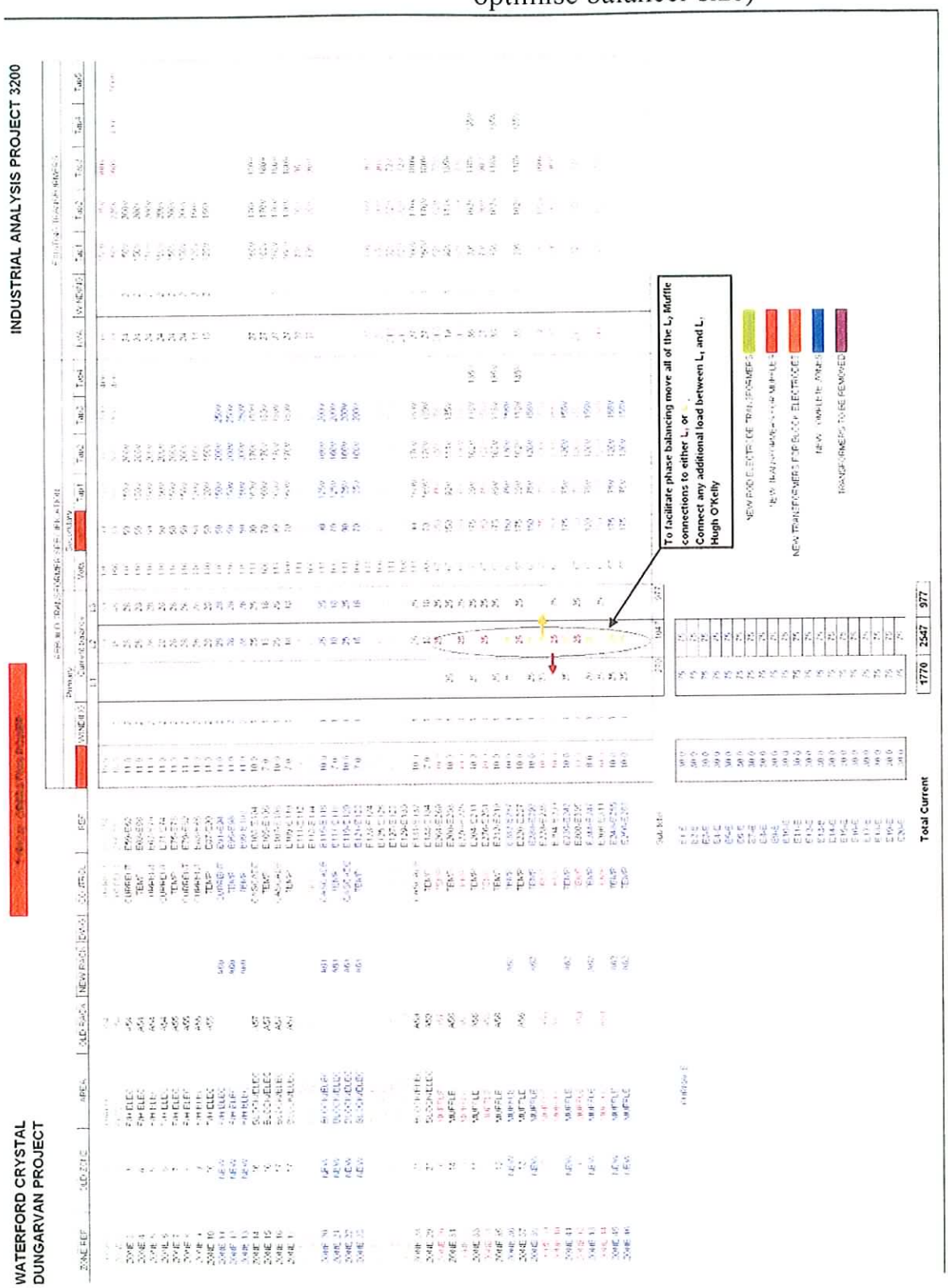


Main Supply Circuit-Breaker and Amp-Meters

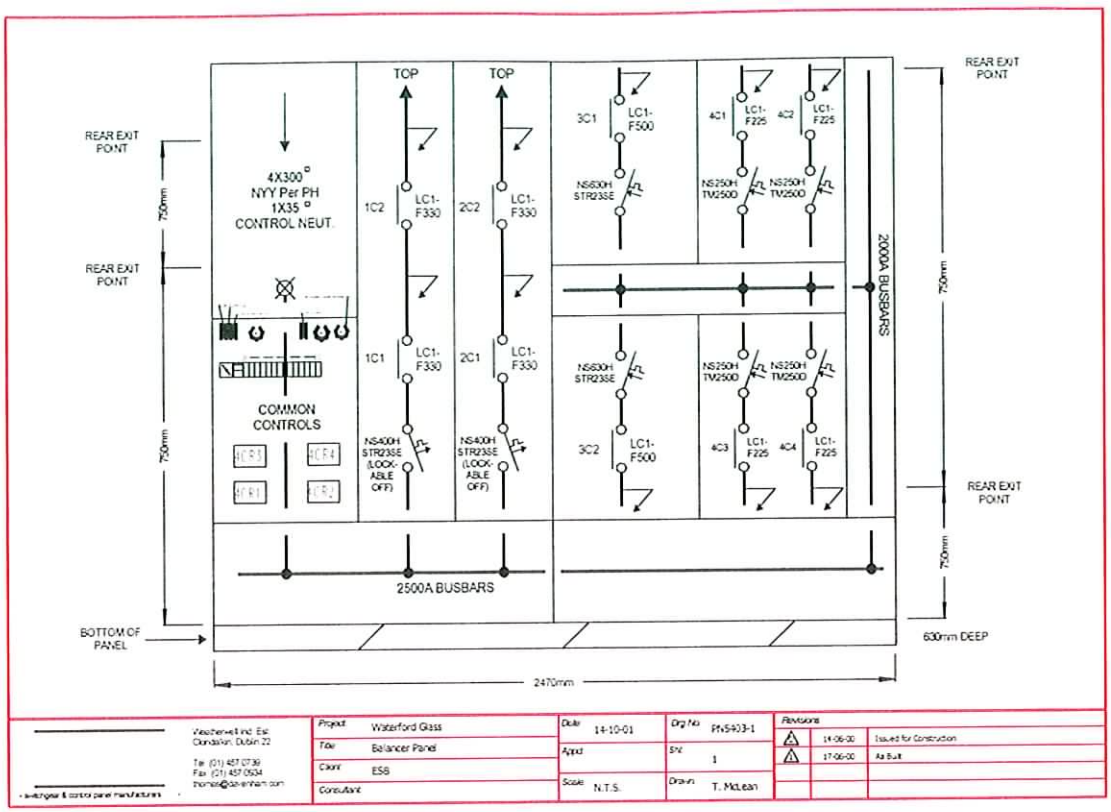
Appendix F Production Motor Balancer Test Results on Mains

Appendix G Motor Balancer Test Results -- Standby Generator

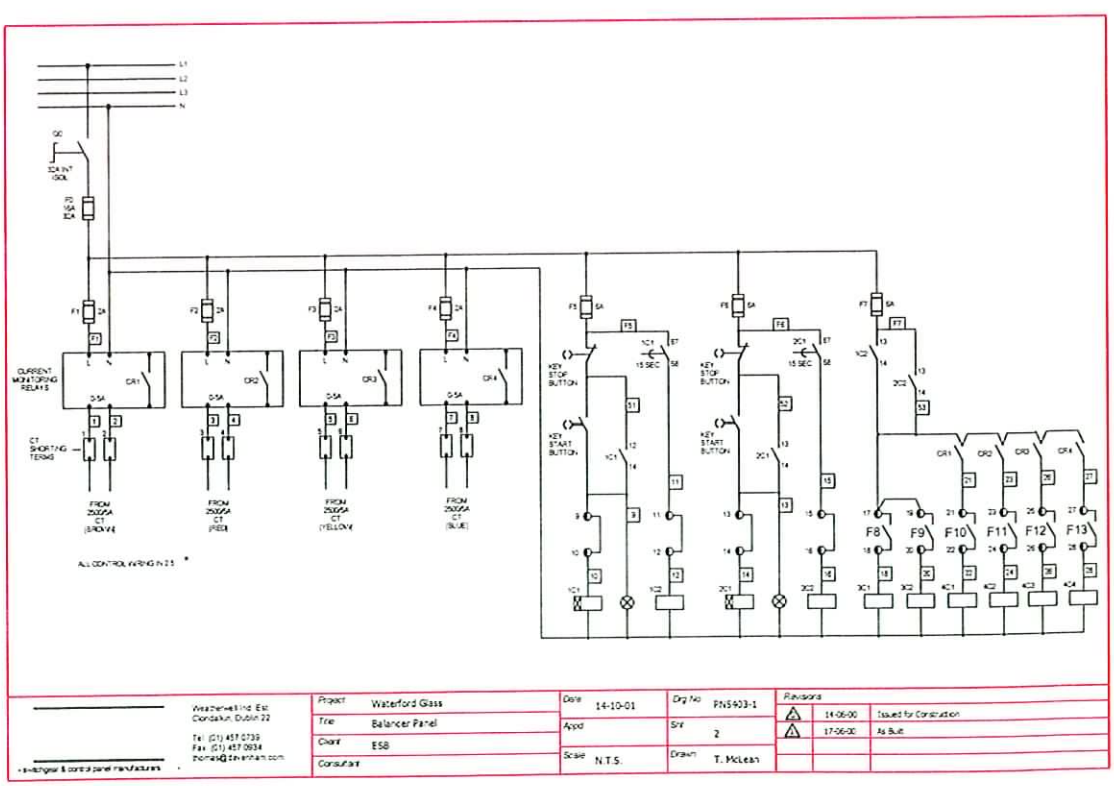
Appendix H Furnace Heating Zones (arrangement to optimise balancer size)



Appendix I Wiring Diagram for Inductor/Capacitor Balancer.

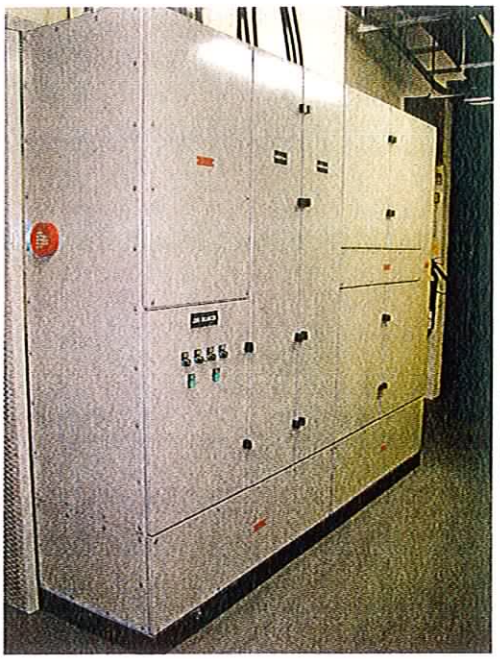


Power Circuit Wiring Diagram



Control Circuit Wiring Diagram

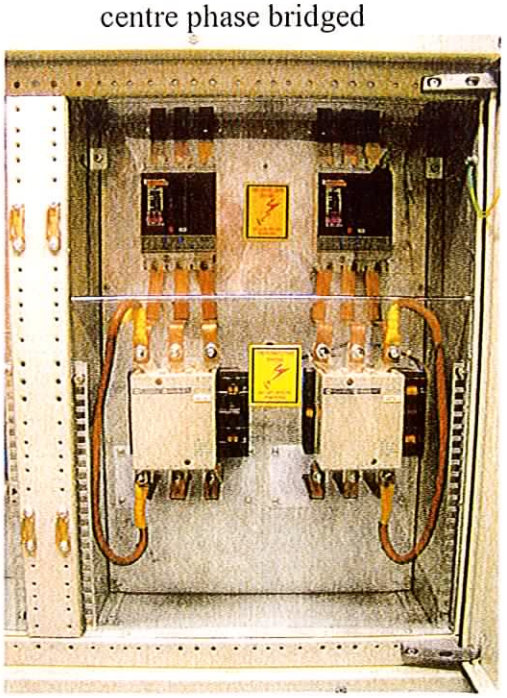
Appendix J Capacitor/Inductor Balancer Photographs.

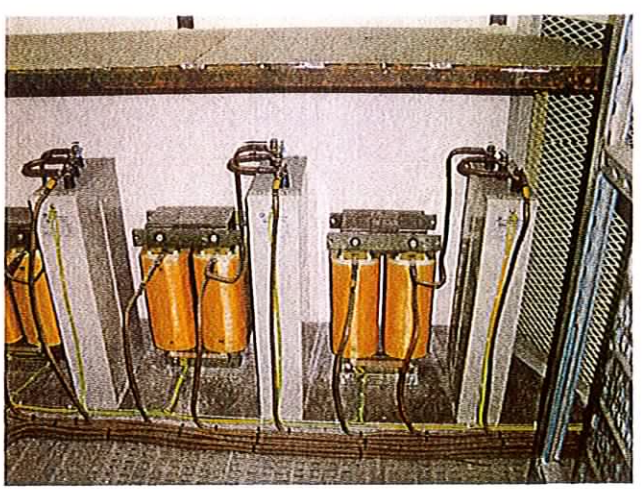


Balancer Switchboard

Capacitor/Inductor Units

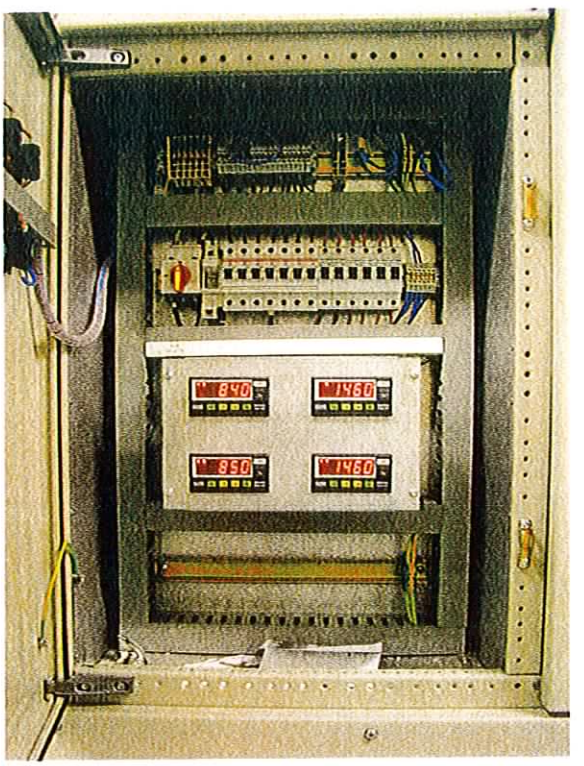
Controlling Contactors showing centre phase bridged





Capacitor/Inductor Units

Step Controlling Relays



View of Caged Capacitor/Inductor Compound

Appendix K Capacitor Voltage Stress Calculation (worst case).

The result below produced by the balancer programme appendix A, shows the effect of disconnection the centre phase form the larger of the two balancers, with all steps in and no furnace load connected. The capacitor voltage reaches 887 V, at which level the main circuit-breaker trips on overvoltage (setting 660 V). These capacitors have a rating of 600 (+10%) volts continuous and a short term over-voltage rating of 1000 volts

Inputs:-

VRS =400, VR1S1 =399.785

XL =(0, 0.24492), XC =(0, -0.24492)

Z1 =(0.066, 1.83), Z2 =(0.031, 0.15)

ZS =(0.00138, 0.00733), ZL=(0.3182, 0)

Results:-

A=0 B=0

Pilot motor Irp=92.7926, Isp=163.342, Itp=130.396

System IR =845.549 at pf =0.326425

System IS =763.313 at pf =0.450463

System IT =1596.6 at pf =0.997283

%Vnps =2.78243

Auto transformer

I AV =163.342, KVA AV =0

I Mid =0, KVA Mid =0

I BV =92.7926, KVA BV =0

Voltage T removed, VC =887.293, VL = 499.384

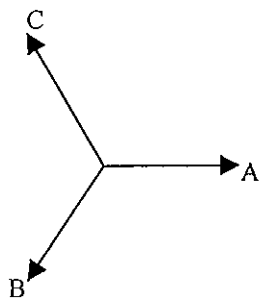
Capacitor KVAR = 653.275, Inductor mH = 0.779605

Go again? Yes = Space_bar / No = any other key :

Appendix L L/C Balancer Test Off-Load on Standby Generator

TEST OF DUNGARVAN BALANCER ON 2.5 MVA TRAFO WITH NO LOAD CONNECTED.
VOLTAGE VECTOR DIAGRAMME AND CALCULATED CHANGE IN % Vnps.

a) Result with 2 number 132kW motors running on no load



A = 234 @ 000°
B = 234 @ 240°
C = 233 @ 120°

∴ %Vnps = 0.14

b) Result with 2 number 132kW motors running on no load + capacitor inductor balancing for 1257 Amps total (larger balancer with all steps switched in).

Note: 2 phases of a 122.5 (120) kVAr, 600V capacitor gives 90.74 Amps at 400V,
or sqrt 3 X 90.74 = 157.17 Amps of single phase load balancing.
8 steps balances 1257 Amps of single phase load.
Let the steps be 3,3,1,1.
Reactor sizes are 4.67mH, 14.03mH

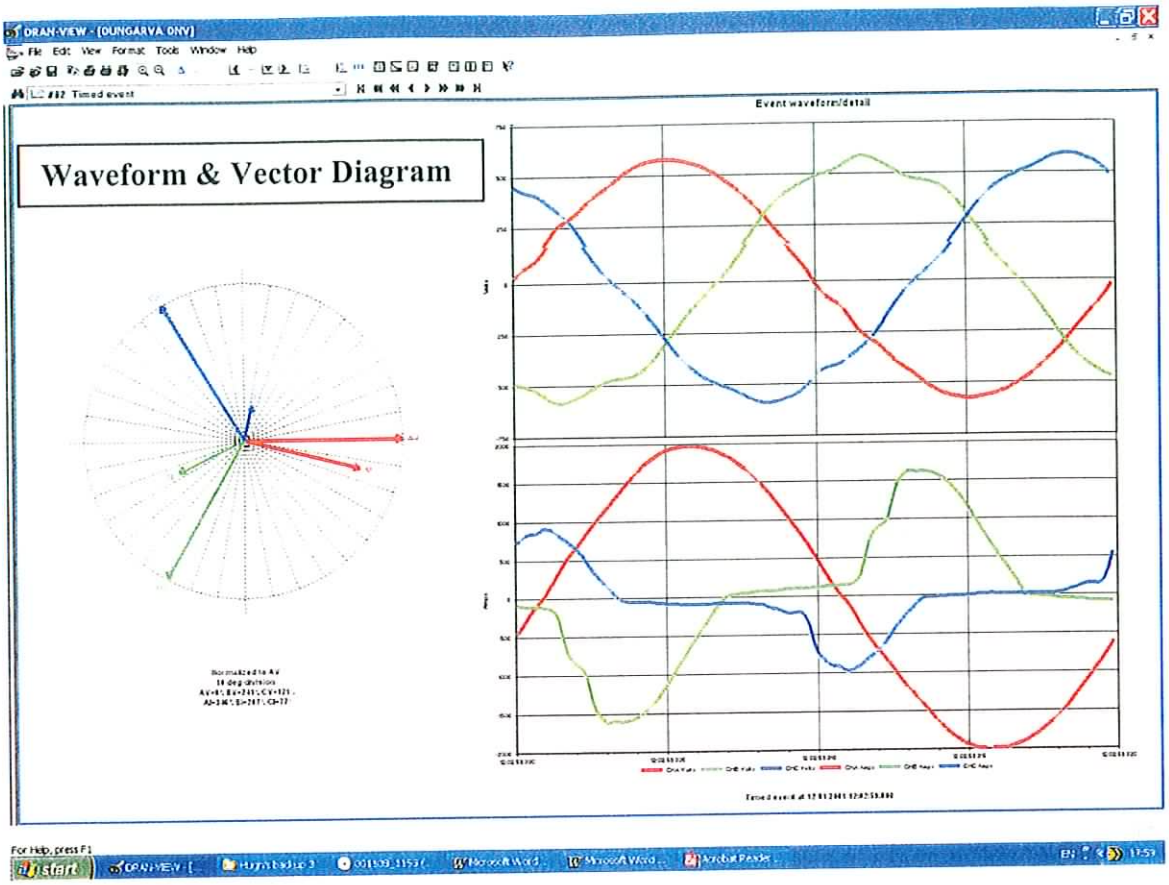
A = 229 @ 000°
B = 240 @ 239°
C = 232 @ 117°

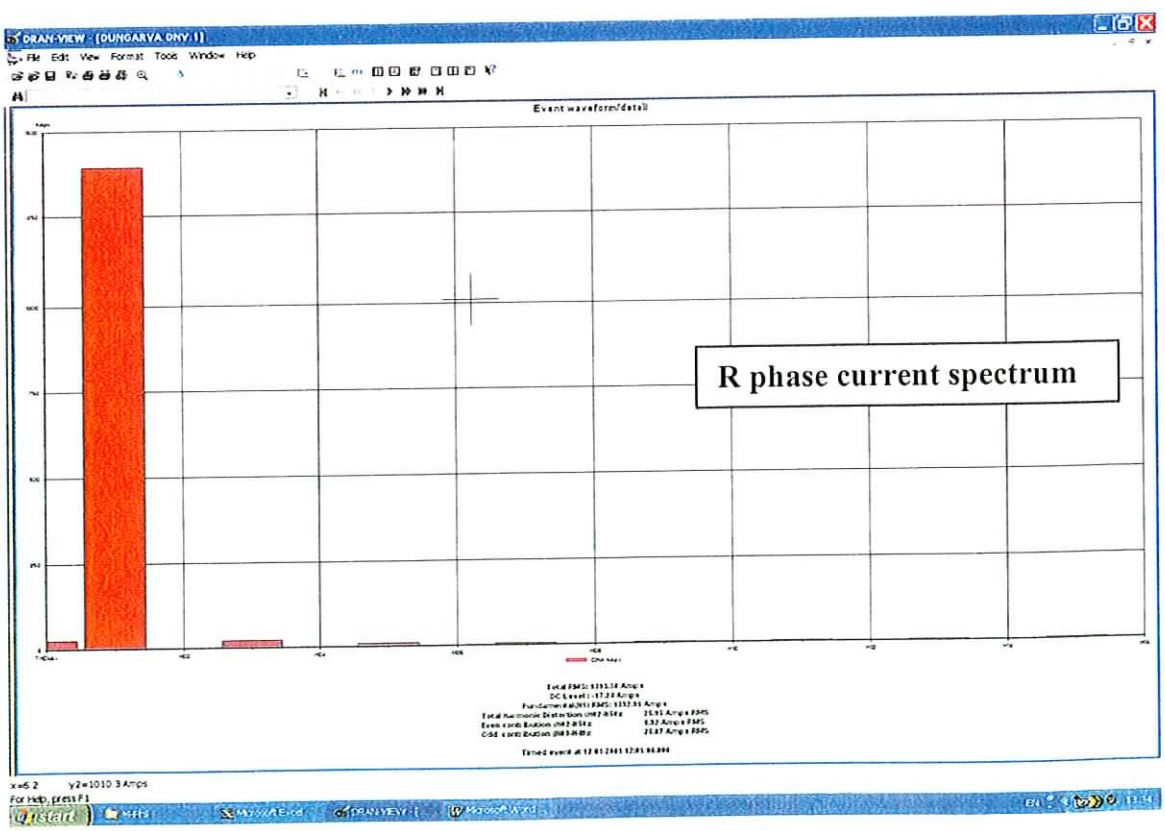
∴ %Vnps = 2.94

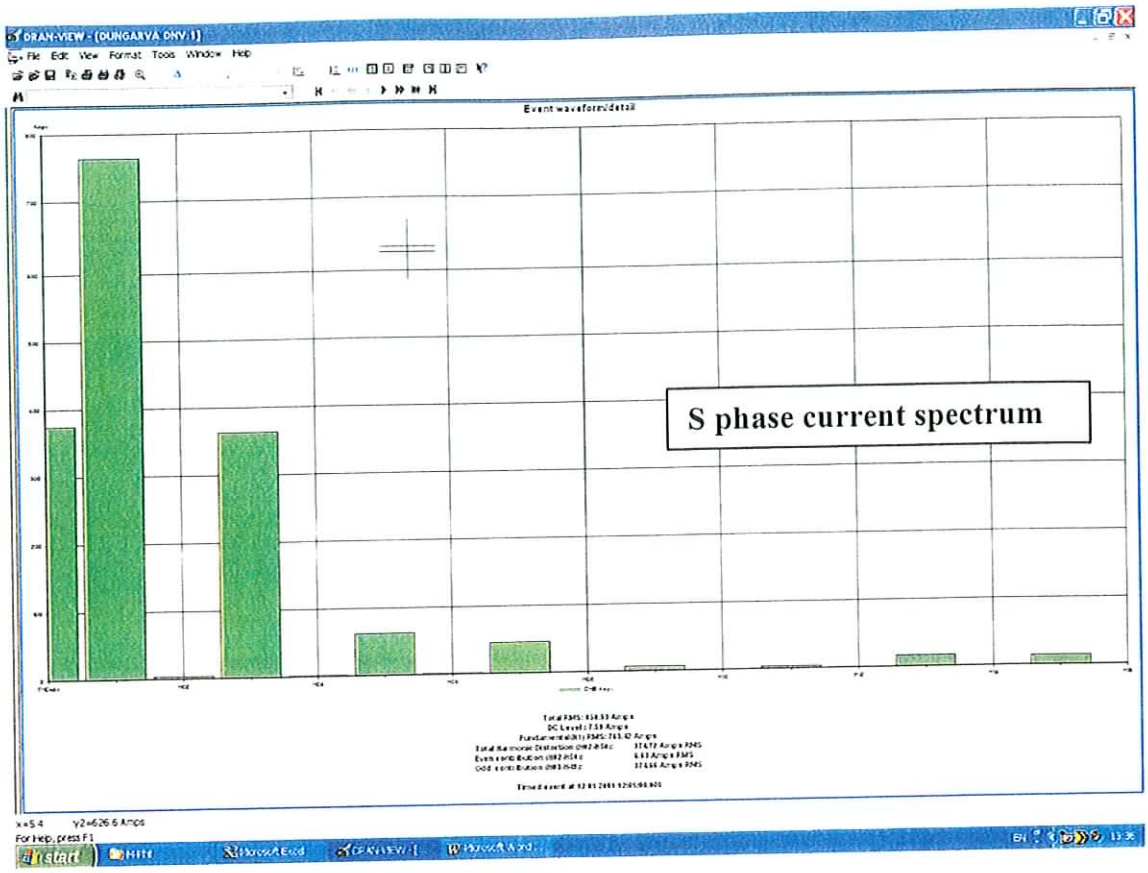
Appendix M Calculated %Nps with No-load and all Steps Switched-In on Balancer R-S

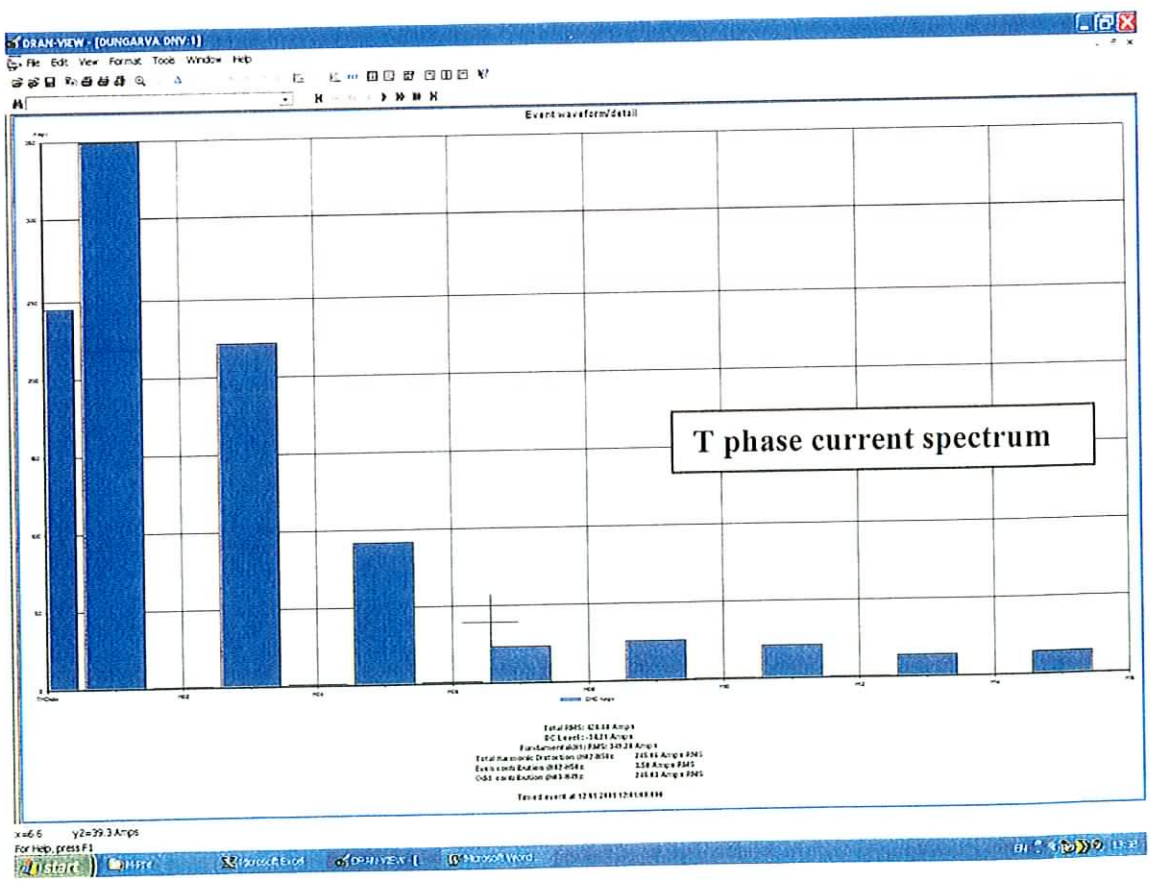
Effect of two phase load on voltage unbalance	
enter data in orange, answer in blue	
2 Phase Load kVA	290.27
Power factor	0
Voltage	400
Amps	725.675
I_R	725.675
I_2	362.8375+209.484328297091i
I_{R2}	362.8375+209.484328297091i
I_{S2}	-362.8375+209.484328297091i
I_{T2}	2.27373675443232E-013+418.968656594182i
I_1	362.8375-209.484328297091i
I_{R1}	362.8375-209.484328297091i
I_{S1}	-362.8375-209.484328297091i
I_{T1}	2.27373675443232E-013+418.968656594182i
Calculated Short Circuit Power (MVA) at Trafo LV terminals	9.69
R/X ratio	0
Z	0.016511868
X	0.016511868
R	0
Z complex	1.65118679050568E-002i
Delta V1	3.45897755702112+5.99112487100105i
Delta V2	-3.45897755702112+5.99112487100105i
Delta VR	11.9822497420021i
Delta VS	-11.9822497420021i
Delta VT	5.32907051820076E-015i
Balanced Voltage Vrs	400
Balanced Voltage Vst	-200-346.410161513776i
Balanced Voltage Vtr	-200+346.410161513776i
Unbalanced Voltage Vrs	400+23.9644994840042i
Unbalanced Voltage Vst	-200-358.392411255778i
Unbalanced Voltage Vtr	-200+334.427911771774i
Positive Phase Seq V	203.458977557022-109.478928966924i
Absolute V_1	231.0437003
Negative Phase Seq V	-3.45897755702087-5.9911248710013i
Absolute V_2	6.917955114
% NPS Voltage	2.99%

Appendix N Load Current, Furnace Only






DRAN-VIEW - [DUNGARVA DNV: 1]
File Edit View Format Tools Window Help
Event waveform/detail
S phase current spectrum
For Help, press F1


DRAN-VIEW - [DUNGARVA DNV: 1]
File Edit View Format Tools Window Help
Event waveform/detail
T phase current spectrum
For Help, press F1

Measured Harmonic Voltages and Currents (furnace load only)

	CHA Volts (RS)	CHB Volts (ST)	CHC Volts (TR)	CHA Amps (RS Phase)	CHB Amps (ST Phase)	CHC Amps (TR Phase)
FND	401.16	403.76	403.07	1392.9	763.42	349.28
H02	0.11	0.21	0.15	0.7	3.8	0.85
H03	10.83	10.55	6.13	21.3	363.83	221.69
H04	0.14	0.35	0.22	0.6	2.3	1.52
H05	3.77	0.92	2.86	9.5	63.14	91.54
H06	0	0.5	0.51	0.5	2	1.22
H07	0.95	14.84	13.82	5.1	46.45	23.36
H08	0.11	0.21	0.15	0.4	1.3	0.67
H09	1.83	3.6	2.47	4.8	7.19	25.68
H10	0.07	0	0.07	0.5	0	0.91
H11	1.87	1.56	0.63	4.4	4.2	21.28
H12	0.14	0.06	0.15	0.2	0.9	0.98
H13	2.47	1.25	1.86	4.5	16.48	13.84
H14	0.07	0.12	0.02	0.2	1.2	0.67
H15	3.03	1.12	1.98	4	14.39	14.33

Power Factor FND	RS phase 0.970 Lagging	ST phase 0.827 Lagging	TR phase 0.721 Lagging

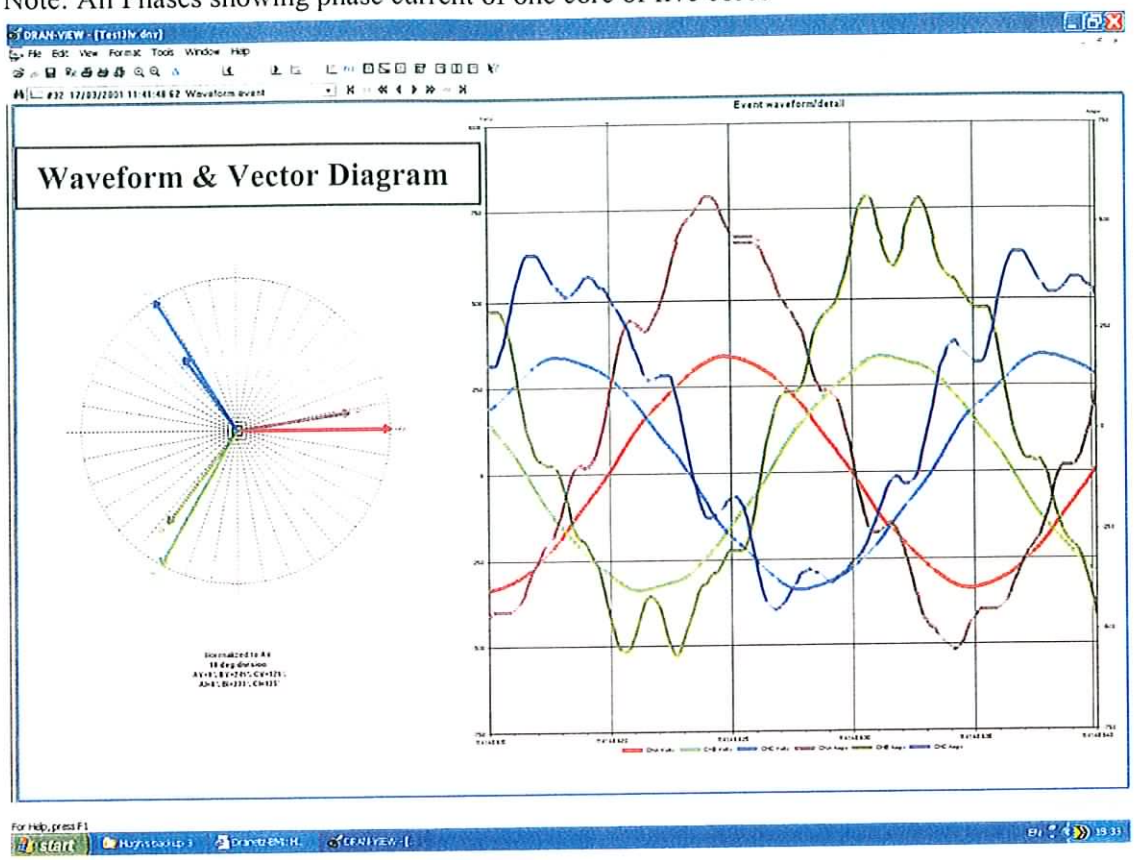
Irs = 1395 angle 346
Ist = 842 angle 207
Itr = 429 angle 77

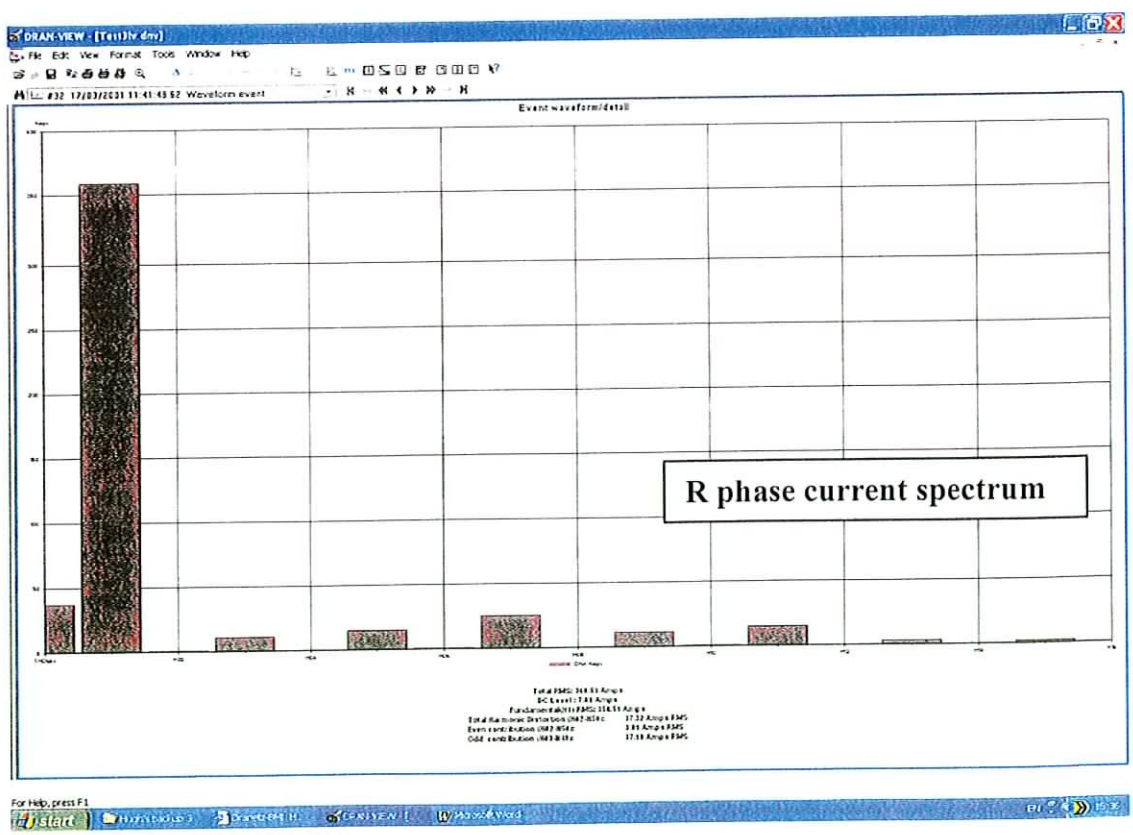
Therefore
Ir = Irs – Itr = 1467 angle 329
Is = Ist – Irs = 2113 angle 181.34
It = Itr – Ist = 1175 angle 43.24
Calculated Inps% = 40.49 (as shown below)

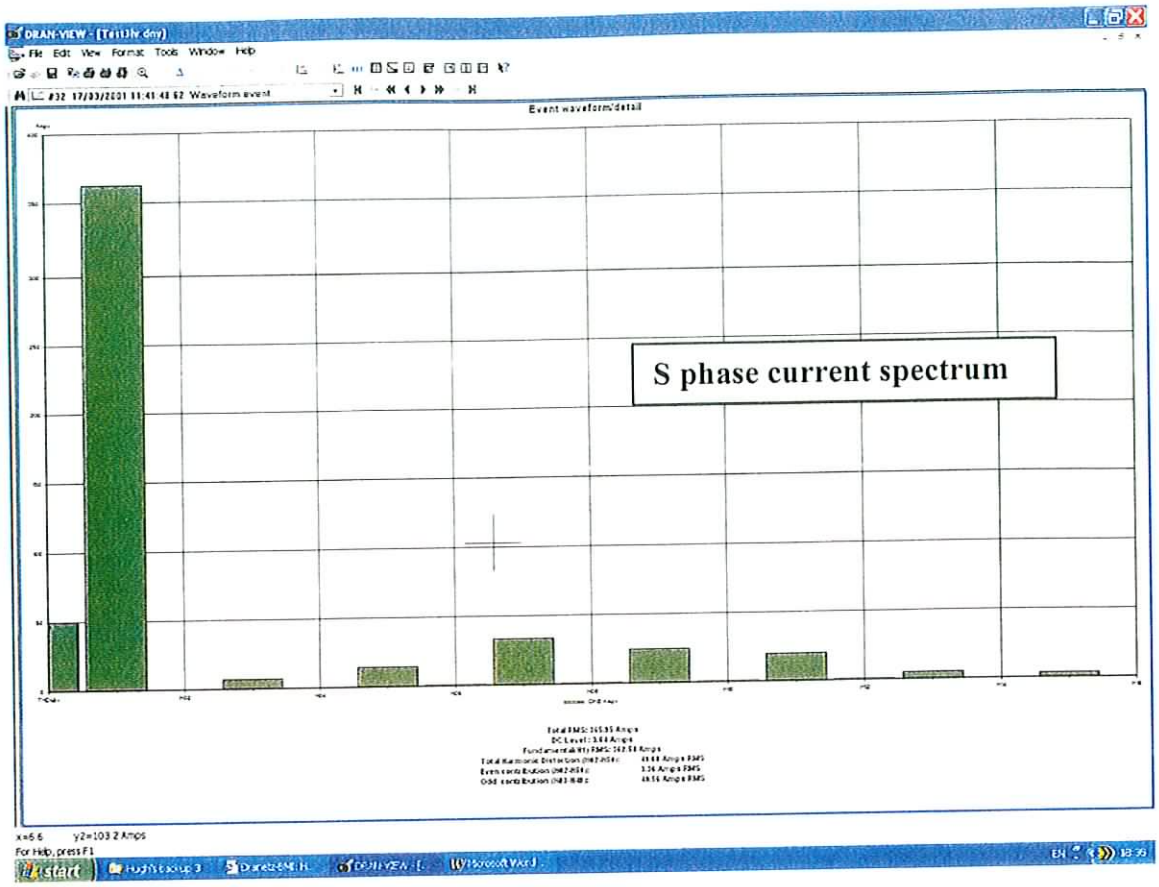
VOLTAGES	magnitude	angle		I component	J component
Phase A	xx	xx		#VALUE!	#VALUE!
Phase B	xx	xx		#VALUE!	#VALUE!
Phase C	xx	xx		#VALUE!	#VALUE!
CURRENTS					
Phase A	1467	329		1257.46443	-755.5608559
Phase B	2113	181.34		-2112.42215	-49.41309663
Phase C	1175	43.24		855.9763913	804.9406298
	1585				
Positive phase seq. impedance	#VALUE!				
Negative phase seq. impedance	#VALUE!				
% NPS Volts	#VALUE!				
% NPS Current	40.49%				

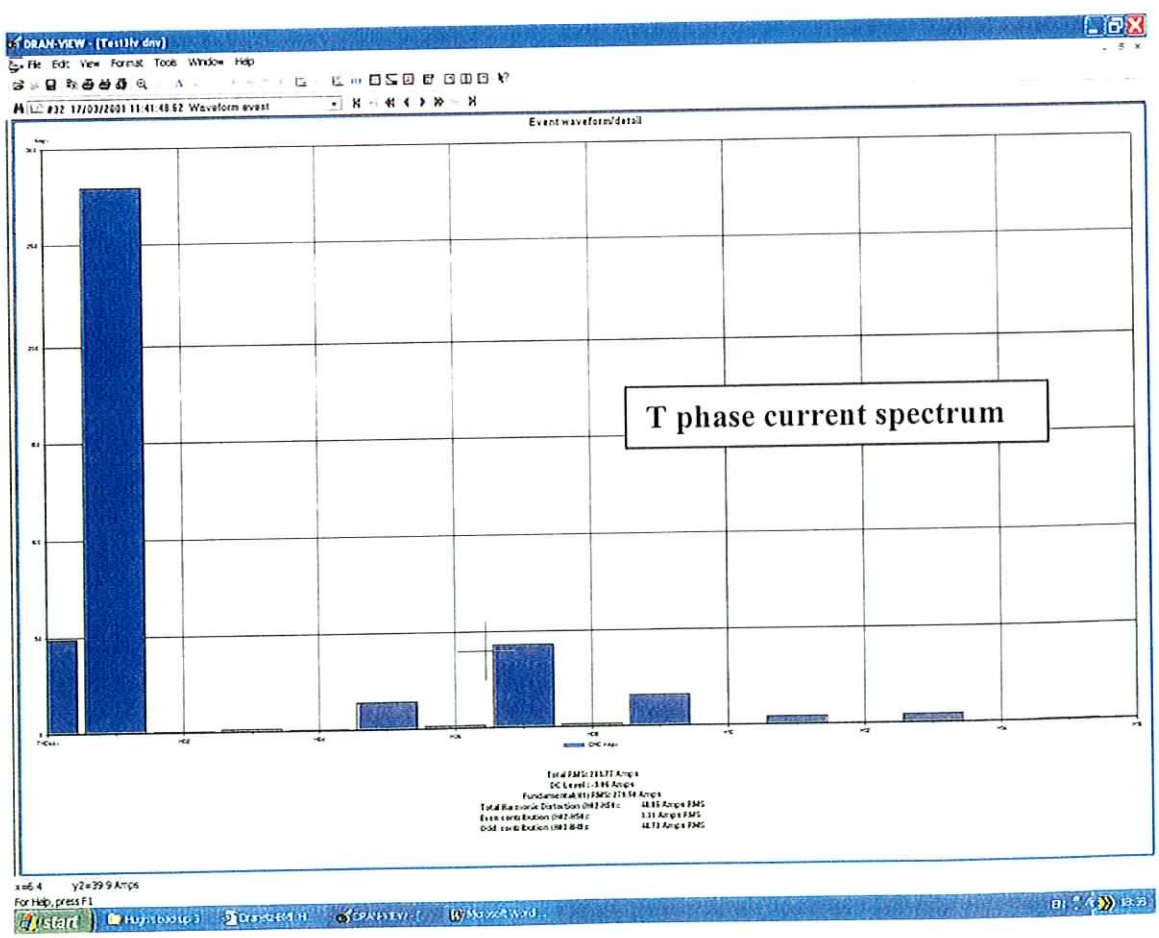
Appendix O Load Current, Furnace plus L/C Balancer

Note: All Phases showing phase current of one core of five cores






DRAN-VIEW - [Test1hr.dmv]
File Edit View Format Tools Window Help
Event waveform/detail
S phase current spectrum
For Help, press F1


DRAN-VIEW - [Test1hr.dmv]
File Edit View Format Tools Window Help
Event waveform/detail
T phase current spectrum
For Help, press F1

Measured Harmonic Voltages and Currents (furnace + balancer)

	CHA Volts	CHB Volts	CHC Volts	CHA Amps	CHB Amps	CHC Amps
FND	235.1	236.49	235.71	1792.55	1812.7	1397.5
H02	0.07	0.05	0.04	6.05	3.55	3.3
H03	1.96	0.95	1.62	54.9	35.15	7.9
H04	0.01	0.04	0.11	2.2	2.85	4.2
H05	1.73	1.42	2.19	74.95	71.5	72.2
H06	0.14	0.16	0.28	5.85	5.7	7.5
H07	2.47	3.51	4.64	127.25	168.55	214.8
H08	0.03	0.1	0.17	2.65	4.8	8.2
H09	0.84	0.98	1.49	57.65	123.25	81.75
H10	0.06	0.05	0.06	5.75	5.35	2.1
H11	0.79	1.48	0.5	75.85	100.7	21.95
H12	0.02	0.01	0.04	3.45	4.8	1.6
H13	0.2	0.32	0.24	16.4	25.25	23.6
H14	0.03	0.05	0.03	1.95	2.7	0.5
H15	0.28	0.47	0.34	9.05	16.8	4

	R phase	S phase	T phase
Power Factor	0.990 Leading	0.992 Leading	0.998 Lagging

Ir = 1819.5 angle 8
Is = 1801.5 angle 233
It = 1410.0 angle 125

Calculated Inps% = 16.18 (as shown below)

VOLTAGES	magnitude	angle		I component	J component
Phase A	xx	xx		#VALUE!	#VALUE!
Phase B	xx	xx		#VALUE!	#VALUE!
Phase C	xx	xx		#VALUE!	#VALUE!
CURRENTS					
Phase A	1819.5	8		1801.792751	253.2254572
Phase B	1801.5	233		-1084.16976	-1438.741871
Phase C	1410	125		-808.742775	1155.004382
	1677				
Positive phase seq. impedance	#VALUE!				
Negative phase seq. impedance	#VALUE!				
% NPS Volts	#VALUE!				
% NPS Current	16.18%				

Appendix P Harmonic Filter Design Programme & Results

PROJECT: Warterford Crystal furnace , Dungarvan -- supplied from standby generator

Branches

	BRANCH 1	BRANCH 2	BRANCH 3	BRANCH 4
Tuning Frequency	148	248	348	448
Operating voltage Vn	400	400	400	400
Capacitor voltage	690	690	690	690
Capacitor power	100	200	400	350
Inductor resistance	0.01	0.01	0.01	0.01
Henry's required per phase mH	1.7297	0.3080	0.0782	0.0539

System

Supply Voltage Vs (kV)	10
R referred to Vs	0
Xl referred to Vs	10.3125
R at Vn	0
Xl at Vn	0.0165
System mH	0.05252

Absorbtions in Amps

	Generated	BRANCH 1	BRANCH 2	BRANCH 3	BRANCH 4	Total		System Amps
Fundamental		54.76	101.12	198.11	171.91	525.90		
3rd	6.05	3.90	0.34	0.53	0.43	2.65	3rd	3.49
5th	54.9	0.39	54.85	5.99	3.69	50.37	5th	8.40
7th	214.8	0.69	6.38	211.40	28.21	212.26	7th	18.65
9th	123.25	0.27	1.94	13.15	116.53	120.99	9th	7.92
11th	100.7	0.63	4.14	21.60	55.23	81.49	11th	19.33
13th	25.25	0.20	1.25	5.91	11.62	18.98	13th	6.29
17th	17	0.16	0.94	4.07	6.79	11.96	17th	5.04
19th	0	0.00	0.00	0.00	0.00	0.00	19th	0.00
						170.22		
Total Branch Amps		55	115	291	217			
Total Branch Rating		84	167	335	293			
Branch Capacitor Voltages (DELTA)		465	469	482	462			

Power factor ratings

Branch kVAr at 50Hz		38	70	137	119	Total kVAr at 50Hz	364

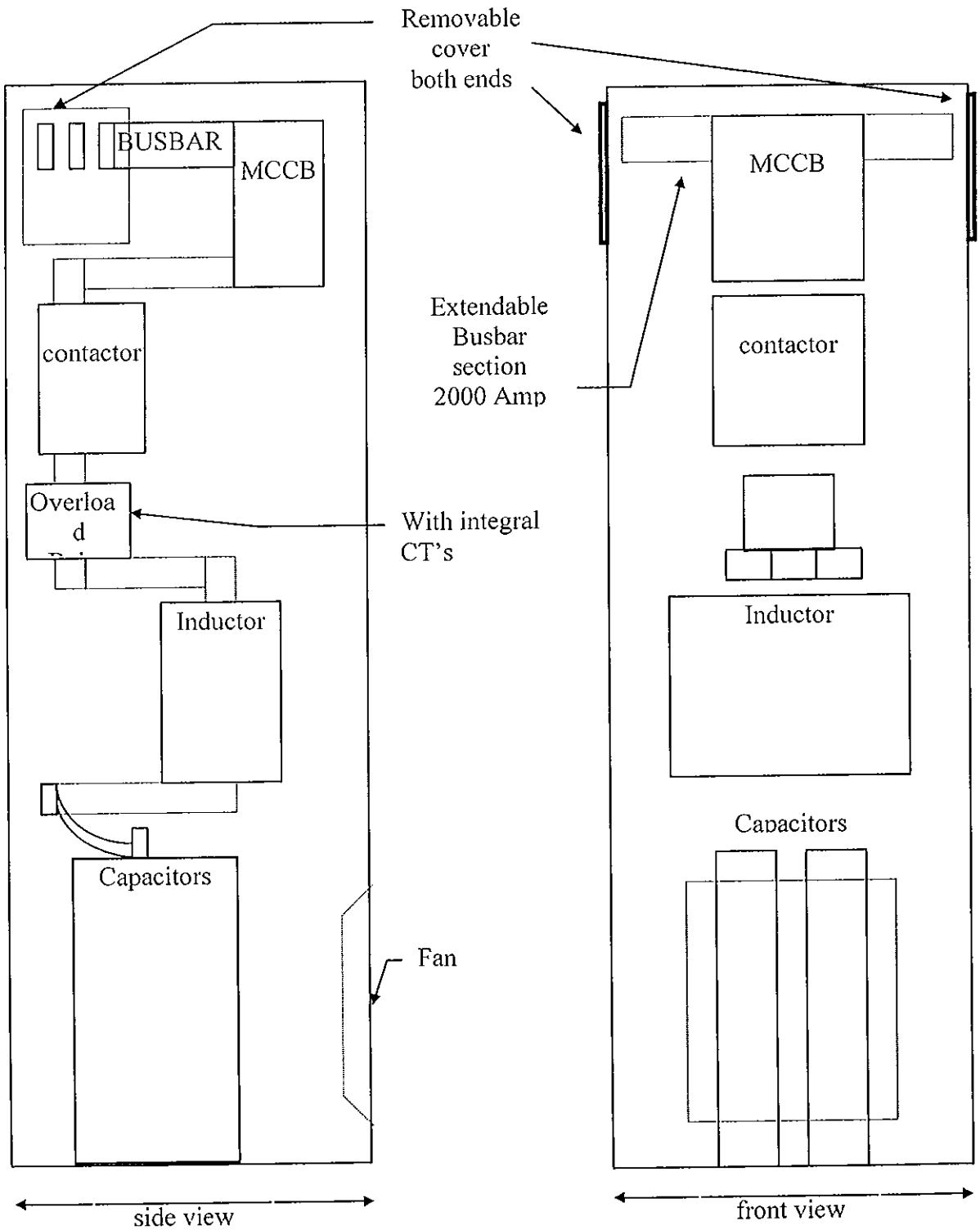
Distortion V%

Fundamental	Unfiltered		Filtered
3rd	0.13		0.07
5th	1.96		0.30
7th	10.74		0.93
9th	7.93		0.51
11th	7.91		1.52
13th	2.35		0.58
17th	2.06		0.61
19th	0.00		0.00
Vthd	15.95%		2.06%

Resonances Hz

Notes: 1. Enter desired values in yellow cells -- all others are calculated
2. To switch a filter branch off enter a very large value of inductor resistance
3. To see impedance profile of supply system plus filter press page-down

Appendix Q Harmonic Filter Construction Diagram



REFERENCES

[1] IEC, Document 60034-1, 'Rotating Electrical Machines part 1: Rating and Performance, revision 3' 1969.

[2] National Standards Authority, EuroNorm standard 50160, 'Voltage Characteristics of Electricity Supplies by Public Distribution Systems', 1995.

[3] Heathcoat, M.: 'J & P Transformer Book 12th edition', Newnes, 1998.

[4] Siemems, 'Siemens SIPCON catalogue SR 10.5', 1998.

[5] Campbell, W.J.: 'Improvements in and Relating to Rotary Phase Converters'. U.K. Patents no. 160 4921, Irish Patent no. 44626, 1971.

[6] Kemp, P.: 'A.C. Current Electrical Engineering', Macmillan, 1963.

[7] Electricity Association UK, Engineering Recommendation G5/4, 'Planning Levels for Harmonic Voltage Distortion and Connection of Non-Linear Equipment to Transmission Systems and Distribution Networks', 2001.

[8] Wildi, T.: 'Electrical Machines, Drives, and Power Systems, 3rd edition', Prentice Hall, 1997.

[9] McLyman, Colonel Wm. T., 'Transformer and Inductor Design Handbook, 2nd edition', Marcel Dekker, Inc., 1988.

[10] Say, M. G., 'Performance and Design of Alternating Current Machines, 3rd edition', Sir Isaac Pitman & Sons Ltd, 1968.

[11] Richardson, D.V., Caisse A.J.: 'Rotating Machinery and Transformer Technology, 4th edition', Prentice Hall, 1997.

[12] Bogart, T.F.: 'Electric Circuits', Macmillan/McGraw-Hill, 1992.

[13] Shepard, J., Morton, A.H., Spence, L.F.: 'Higher Electrical Engineering', Longman, 1995.

[14] Blazer-Boehle-Haneke-Kaiser-Pöhlman-Tetenborn-Vob, 'ABB Switchgear Manual Published by ABB Calor Emag og Germany', 9th Edition 1992.

[15] IEC, Document 61000-3-2 (2001-10), 'Electromagnetic compatibility (EMC) - Part 3-2: Limits - Limits for harmonic current emissions (equipment input current <= 16A per phase)', 2000.

[16] Dranetz-BMI, Edison, New Jersey 08818 USA, www.dranetz-bmi.com

[17] IEC/TR3, Document 61000-3-6 (1996-10), 'Electromagnetic compatibility (EMC) - Part 3: Limits - Section 6: Assessment of emission limits for distorting loads in MV and HV power systems - Basic EMC publication', 1996.

[18] IEC, Document 61000-4-7 (2002-08), 'Electromagnetic compatibility (EMC) - Part 4-7: Testing and measurement techniques - General guide on harmonics and inter-harmonics measurements and instrumentation, for power supply systems and equipment connected thereto', 1991.

[19] Ciletti, M.D.: 'Circuit Analysis and Design', Holt Rinehart and Wilson Inc., 1988.

[20] Chen, W.K.: 'The Circuit and Filters Hanbook', CRC & IEEE Press, 1995.

[21] Blinchikoff, H.J. & Zverev, A.I.: 'Filtering in the Time and Frequency Domains', John Wiley & Sons, 1976.

[22] Johnson, D.E., Johnson, J.R., Hilburn, J.L., Scott, P.D.: 'Electrical Circuit Analysis', Prentice Hall, 1997.

[23] Sedra, A.S., Brackett, P.O.: 'Filter Theory and Design, Active and Passive', Matrix Publishers, 1978.

[24] Mouthaan, T.: 'Semiconductor Devices Explained', John Wiley & Sons, 1999.

[25] Wells, R.: 'Solid State Power Rectifiers', Granada Publishing, 1982.

[26] Cunningham, D. R.: 'Circuit Analysis', Houghton Mifflin Company, 1995.

[27] Bozic, S.M., Cheng, R.M.H., Parsons, J.D.: Electronic and Switching Circuits', Edward Arnold, 1975.

[28] Vlach, J., Singhal, K.: 'Computer Modelling Methods for Circuit Analysis and Design', Van Nostrand Reinhold, 1994.

[29] Roberts, G.W., Sedra, A.S.: 'Spice', Oxford University Press, 1997.

[30] Behforooz, A., Hudson, F.J.: 'Software Engineering Fundamentals', Oxford University Press, 1996.

[31] Arnush, C.: 'Teach Yourself Turbo C++4.5 for Windows', Sams Publishing, 1995.

[32] Antonakos, J.L., Mansfield, K.C.: 'Structured C for Engineering and Technology', Prentice Hall, 2001.

[33] Reverchon, A., Ducamp, M.,: 'Mathematical Software Tools in C++', John Wiley & Sons, 1993.